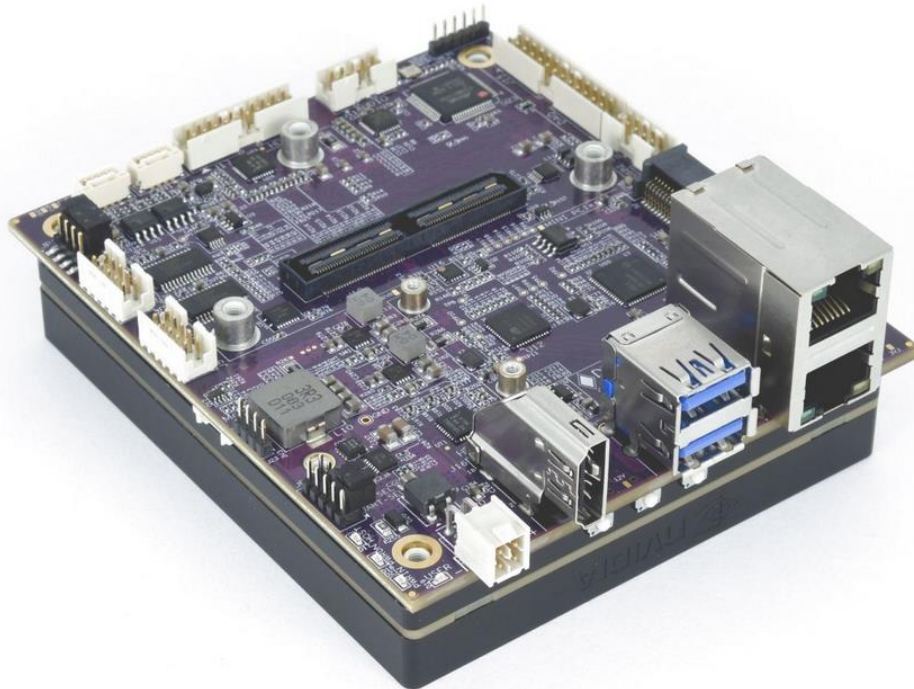




STEVIE™

Carrier for NVIDIA® AGX Xavier Module

USER MANUAL



Revision No	Release Date	Comments
1.01	08/05/2019	Initial Release
1.02	02/25/2020	Major Feature Updates. Added Section: Getting Started
1.03	03/27/2020	Added Addendum
1.04	12/04/2020	Updated details based on Rev A board
1.05	06/02/2021	Updated based on Rev B board for FAN connector
1.06	09/22/2021	Updated Available models and Block Diagram

**FOR TECHNICAL SUPPORT
PLEASE CONTACT:**

Email: support@diamondsystems.com

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1 IMPORTANT SAFE HANDLING INFORMATION



WARNING!

ESD-Sensitive Electronic Equipment

Observe ESD-safe handling procedures when working with this product.

Always use this product in a properly grounded work area and wear appropriate ESD-preventive clothing and/or accessories.

Always store this product in ESD-protective packaging when not in use.

Safe Handling Precautions

Diamond Systems boards are designed with complex circuitry and electronic components that are ESD-sensitive. This increases the likelihood of the boards incurring accidental damage during handling, installation, and connection to other equipment.

It is highly recommended that the following precautionary measures and best practices be observed in sequential order:

- Wear an anti-static Wristband/Strap or/and an antistatic Lab Coat or/and Rubber-soled shoes.
- Spread anti-static mats over the table or work surface or/and anti-static mats on the floor.
- Unpack components and remove them from their anti-static bags only when they are ready to be used.
- Avoid ungrounded surfaces such as plastic, carpets, floors, or tables, in the work area.
- Handle boards by the edges and their metal mounting brackets. Avoid touching components on the boards and the edge connectors that connect to expansion slots.

The following information describes common causes of failure found on boards and components returned to Diamond Systems for repair. It is provided as a guideline to avoid accidental damage.

ESD Damage: This type of damage is typically impossible to detect because there is no visual sign of failure or damage. In this type of damage, the board eventually stops functioning because of some defective components. Usually, the failure can be identified, and the chip can be replaced.

To prevent ESD damage, always follow proper ESD-prevention practices when handling computer boards.

Damage During Handling or Storage: Physical damage on boards also occur due to mishandling. A common observation is that of a screwdriver slipping on the board during installation, causing a gouge on the PCB surface, cutting signal traces or damaging components.

Another common observation is damaged board corners, indicating the board was dropped. This may or may not cause damage to the circuitry, depending on components located near the edges. Most Diamond System boards are designed with a minimum 25 mils clearance between the board edge and component pad. The ground/power planes are located a minimum of 20 mils from the edge to avoid possible shorting from this type of damage. However, these design rules do not prevent damage in all situations.

Sometimes boards are stored in racks with slots that grip the edge of the board. This is a common practice for board manufacturers. Though Diamond Systems boards are resilient to damages, the components located close to the board edges can be damaged or even knocked off the board if the board lies tilted in the rack.

Diamond Systems recommends that all its boards be stored only in individual ESD-safe packaging units. If multiple boards are stored together, they should be contained in bins with dividers placed between the boards. Do not pile boards on top of each other or cram too many boards within a small location. This can cause damage to connector pins or fragile components.

Damage During Installation in a PC/104 Stack: Damage on boards can also occur while installing the board in a PC/104 Stack. A common cause of damage occurs when the connector pins are misaligned with their corresponding interfaces on the stack.

For example, during installation, if a PC/104 board pin-mapping is misaligned/shifted by 1 row or 1 column, it can cause the $\pm 12V$ power and ground signal lines on the bus to contact the wrong pins on the board and damage components linked to the data bus lines.

Bent Connector Pins: This type of problem can be resolved by re-bending the pins to their original shape using needle-nose pliers.

The most common cause of a bent connector pin is when the board is pulled off a stack by tugging it at angles from one end of the connector to the other, in an effort to release it off the stack. Tugging the board off the stack in this manner can bend the pin(s) significantly.

A similar situation can occur when pulling a ribbon cable off a pin header. If the pins are bent too severely, bending them back can cause them to weaken or break. In this case, the connector must be replaced.

Power Damages: There are various causes of power-specific damages that can occur while handling the board. Some common causes such as –a metal screwdriver tip slipping, or a screw dropping onto the board while it is powered-up, causes a short between a power pin and a signal pin on a component.

These faults can cause over-voltage/power supply problems besides other causes described below.

To avoid such damages, assembly operations must be performed when the system is powered off.

Power Supply Wired Backwards: Diamond Systems power supplies and boards are not designed to withstand a reverse power supply connection. This will destroy almost all ICs connected to the power supply. In this case, the board will likely be irreparable and must be replaced. A chip destroyed by reverse or excessive power will often have a visible hole or show some deformation on the surface due to vaporization inside the package.

Overvoltage on Analog Input: If a voltage applied to an analog input exceeds the power specification of the board, the input multiplexer and/or parts behind it can be damaged. Most Diamond Systems boards will withstand an erroneous connection of up to 36V on the analog inputs, even when the board is powered off, but not on all boards, and not under all conditions.

Overvoltage on Analog Output: If an Analog output is accidentally connected to another output signal or a power supply voltage, the output can be damaged. On most Diamond boards, a short circuit to ground on an analog output will deter any damage to the board.

Overvoltage on Digital I/O Line: If a Digital I/O signal is connected to a voltage above the maximum specified voltage, the digital circuitry can be damaged. The acceptable voltage range, on most Diamond Systems boards connected to digital I/O signals is 0-5V, with overvoltage protection up to 5.5V (-0.5 to 5.5V). Overvoltage beyond this limit can damage the circuitry.

Other considerations are Logic Signals, which are typically generated between 12V to 24V.

If a Digital I/O Line of 12V to 24V is connected to a 5V logic chip, the chip will be damaged, and the damage could extend to other chips in the circuit.

IMPORTANT! Always check twice before Powering Up!

2 INTRODUCTION

2.1 Stevie Baseboard Overview

The Stevie baseboard is the latest product from Diamond Systems to integrate the newly released Standalone NVIDIA AGX Xavier System on Module (SoM) Series:

- AGX Xavier 16GB
- AGX Xavier 32 GB
- AGX Xavier 8 GB

Packaged in an ultra-compact sized form-factor measuring H 3.6" x W 4.13" (92 mm x 105 mm) Stevie baseboard is empowered to deliver the latest technologically innovative breakthroughs by converging Fifth Generation (5G) and Fourth Generation (4G) Networking Technologies.

The Stevie baseboard integrates the AGX Xavier Series Module to offer a full-featured, embedded system that significantly enhances performance, power efficiency, and optimized I/O capabilities, for processing real-time Artificial Intelligence (AI), Machine and Deep Learning and high-level Audiovisual (AV) computing tasks at unconventional speeds.

Feature Description and Connector Type

<i>Feature</i>	<i>Description</i>	<i>Connector Type</i>
Power	12V and/or 9V-20V Wide Input Supply Range	2x2 Samtec IPL1
USB	2x USB 2.0; 2x USB 3.1	2x5 Header, Dual Stack UBS 3.0 Type A
Ethernet	10/100/1000 Mbps through I210 Controller with On-board Magnetics	RJ45 GbE (X2)
	10/100/1000 Mbps through RGMII Interface to KSZ9031 PHY with On-board Magnetics	
Mass Storage	1 Mini-PCI Express (mPCIe) Socket	RA PCIe MiniCard 52 Position (52-Pin-Card-Edge-Type Connector)
	1 M.2 PCIe SSD Socket 2280 (22 mm wide x 80 mm long) NVMe Expansion Slots (4-Lane PCIe Gen 3)	M.2 (Key M) Socket
	1 Universal Flash Storage (UFS) and Micro SD	UFS & Micro SD Push-Pull Type Connector
Audio	Via SGT500 CODEC	2x5 Header
Serial Ports	2 RS-232/422/485 Ports. Software configurable through SP336 Transceivers	2x5 Header
	2 RS-232/422/485 Ports. Software configurable through SP336 Transceivers	2x5 Header
Display	1 HDMI 2.0a/b Routed from the Module	HDMI (Type A)
	1 HDMI 2.0a/b Routed from the Module	2x10 Header
Camera	4 x4 / 8 x2 Lane CSI-2 Camera Interface	2 x 60 Receptacle SMT
Data Acquisition (DAQ)	6x SE ADC Input / 3x DE ADC Input to SAM Controller and 2x DAC via SAM Controller	2x13 Header
Digital I/Os	13 Digital I/O via SAM Controller	
CAN Header	2x CAN	1x4 1.25mm SMD
Utility	PWR_BTN, RESET, FORCE RECOVERY	2x5 Header

Operating System Support

Linux Kernel version 4.4.38; Ubuntu 16.04 AArch64

Mechanical, Electrical and Environmental Properties

Form-Factor H 3.6" x W 4.13" (92 mm x 105 mm)

Cooling Mechanism Conduction Cooling

Power Input Range +9V to +20V, +12V Typical

Operating Temperature Range -25°C to +80°C Ambient

2.2 Stevie Baseboard Models

The Stevie Baseboard includes two variants which are listed in the following table. All variants incorporate the same functionalities and differ only in feature requirements.

<i>Model</i>	<i>Feature</i>
STV-BB01	STEVIE carrier board for AGX Xavier, full feature model
STV-BB02	STEVIE carrier board for AGX Xavier, Single Ethernet port

2.3 AGX Xavier Modules Overview

Measuring L x 3.93" X W 3.42" X H 0.62" (100 mm x 87 mm x 0.02 mm) the AGX Xavier and AGX Xavier 8 Series are autonomous, highly sophisticated, low-powered modules, engineered to process more than 32 and 20 trillion operations per second respectively, at a speed of 56 Gbit per second.

Embedded with 9 billion Transistors and a 699 Neuro-Mezzanine Pin Board-to-Board connector that supports Hi-Speed I/O processing of data including PCI/PCIe Gen 5 and Gen 4 technologies, the modules enable Deep Learning Applications to operate in Small Form-Factor (SFF) products such as Computer-on-Module (COMs), and Smart devices such as Cameras, within a secure and automotive environment.

The circuitry and I/O connectors on the baseboard utilize all available features of the AGX Xavier Series Module to deliver highly versatile performance in industrial environments.

AGX Xavier Series Feature Description

<i>Feature</i>	<i>Description</i>	
	AGX XAVIER	AGX XAVIER 8 GB
GPU	512-core NVIDIA Volta™ GPU with 64 Tensor Cores	384-core NVIDIA Volta™ GPU with 48 Tensor Cores
DL Accelerator	(2x) NVIDIA Deep Learning Accelerator (NVDLA) Engines	(2x) NVIDIA (NVDLA) Engines
CPU	8-core ARMv8.2 @ 64-bit CPU, 8MB L2 + 4 MB L3	6-core Arm@v8.2 64-bit CPU, 6 MB L2 + 4 MB L3
Memory	16 GB 256-bit LPDDR4x 136.5 GB/s	8 GB 256-bit LPDDR4x 85.3 GB/s
Video Encode	2x 1000MP/sec 4x 4K @ 60 (HEVC), 16x 1080p @ 60 (HEVC) 32x 1080p @ 30 (HEVC)	2x 464MP/sec 2x 4K @ 30 (HEVC), 6x 1080p @ 60 (HEVC) 14x 1080p @ 30 (HEVC)
Video Decode	2x 1500MP/sec 2x 8K @ 30 (HEVC), 6x 14k @ 60 (HEVC) 26x 1080p @ 60 (HEVC), 72x 1080p @ 30 (HEVC)	2x 690MP/sec 2x 4K @ 60 (HEVC), 12x 1080p @ 60 (HEVC) 32x 1080p @ 30 (HEVC)
Vision Accelerator	7-way VLIW Processor	7-way VLIW Processor
Camera	16x CSI-2 Lanes (40 Gbps in D-PHY V1.2 or 109 Gbps in CPHY v1.1) 8x SLVS-EC Lanes (up to 18.4 Gbps) Up to 16 Simultaneous Cameras	16x CSI-2 Lanes (40 Gbps in D-PHY V1.2 or 64 Gbps in CPHY v1.1) 8x SLVS-EC Lanes (up to 18.4 Gbps) Up to 16 Simultaneous Cameras
PCIe	5x PCIe Gen4 (16GT/s) Controllers 1x8, 1x4, 1x2, 2x1 PCIe Gen4, Root Port and Endpoint	5x PCIe Gen4 (16GT/s) Controllers 1x8, 1x4, 1x2, 2x1 PCIe Gen3
Storage	32 GB eMMC 5.1	32 GB eMMC 5.1
UPHY	(3x) USB 3.1 (10 Gb/s) (4x) USB 2.0 ports 1 x8 or 1 x4 or 1 x2 or 2 x1 PCIe (Gen4)	3x USB 3.1, 4x USB 2.0 1 x8 or 1 x4 or 1 x2 or 2 x1 PCIe (Gen3)
Connectivity	1 Gigabit Ethernet, MAC, Reduced Gigabit Media Independent (RGMII) Interface	1 Gigabit Ethernet, MAC, Reduced Gigabit Media Independent (RGMII) Interface
Miscellaneous I/O's	UFS, I2S, I2C, SPI, CAN, GPIOs, UART,	UFS, I2S, I2C, SPI, CAN, GPIOs, UART, SD
<i>Mechanical, Electrical, and Environmental Properties</i>		
Form-Factor	H 3.93" x W 3.42" (100 x 87 mm; 16 mm Z-height)	
Weight	280 Grams (9.87 Ounces) +/- 10 grams with Packaging including Thermal Transfer Plate (TTP)	
Connector	699-Pin Board-to-Board Connector	
Cooling Solution	Integrated Thermal Transfer Plate (TTP) with Heat Pipe	
Power Input Range	9.0-20VDC	
Operating Temperature Range	-25°C to +80°C	

3 FUNCTIONAL OVERVIEW

The following section provides functional details of the key sub-systems implemented on the baseboard.

3.1 Processor Modules

The baseboard supports Jetson™ AGX Xavier Series modules.

AGX Xavier Modules integrate 512-core NVIDIA Volta GPU with Tensor Cores and offer 32/16/8 GB of 256-bit LPDDR4x memory with 137 GB/s of bandwidth at 2133 MHz bus speeds that enable AI-powered platform tools to process high-resolution computing tasks at 20 to 32 Tera Operations Per Second (TOPS) respectively.

The modules encapsulate a high-density 699-pin board-to-board connector for breaking out high-speed I/O signals to carrier board systems. This enables the integration of applications and devices across a wide range of products and form-factors.

Four M3 threaded spacers are mounted on the board for installing AGX Xavier module on the bottom side.

3.2 Power Supply Specifications

The baseboard is powered by a regulated 12V supply or wide input voltage range of +9V to +20V power supply.

The maximum permissible reflected ripple measured at the voltage input connector is 50mV p-p.

Power supply voltages for the baseboard are derived from the +9V-20V input source. It is recommended that the power supply unit meet the specified voltage range with additional reserves to support the add-on features listed in the table below.

Power Requirements for Supplementary Features

<i>Feature</i>	<i>12V</i>	<i>5V</i>	<i>3.3V</i>
AGX Xavier Series Module	2.5A		
PCIe MiniCard Socket			2A
M.2 SSD			0.5A
USB 2.0/3.1 Ports (0.5A per USB 2.0 Port and 1A per USB 3.1)		3A	
Camera Circuit		0.2A	0.4A
Second Ethernet Circuit			0.3A
Miscellaneous		1A	1A

3.3 Backup Battery

A 2x1 input connector is provided to enable the use of an external battery for rugged applications.

3.4 Ethernet Ports

The baseboard is equipped with two Gigabit Ethernet ports depends on the models.

1. A 10/100/1000 Ethernet port is derived from the [Intel WGI210IT](#) PCIe Ethernet controller which is accessed via x1 PCIe lane routed from the Module. (**Supported only in STV-BB01 model**).
2. A 10/100/1000 Ethernet port is derived from the RGMII (Reduced Gigabit Media-Independent Interface) output of the Module connected to the on-board [KSZ9031 PHY](#) from Microchip.

GbE ports accommodate the standard RJ45 (Registered Jack) network interface for connecting RJ45/Ethernet cables. The LEDs on the RJ45 serve as an activity indicator to indicate the connectivity, link, speed, and data transmission status across the network.

3.5 Display Controller

The baseboard supports dual HDMI 2.0 a/b Video Output ports.

One HDMI port is routed from the AGX Xavier Series Module and is implemented through the standard HDMI (Type A) connector which uses a 19-pin configuration to transmit audio and video signals.

The second HDMI port is routed from the AGX Xavier Series Module and is implemented through the 2x10 header on the baseboard.

3.6 Camera Serial Interface (CSI)

The AGX Xavier Series Module support four MIPI (Mobile Industry Processor Interface) CSI x4 bricks, enabling a wide array of device types and combinations to be implemented. Up to four 4-lane or six 2-lane or six 1-lane configurations or combinations of camera streams are available. Each lane supports up to 16 Virtual Channels (VC). Each data channel has a peak bandwidth of up to 2.5 Gbps.

The baseboard supports four MIPI CSI x4 camera interfaces through a 120-pin daughterboard connector.

Off-the-shelf add-on Camera Boards from Leopard Imaging/e-con Systems can be plugged into the daughterboard connector to support the four 4-lane or six 2-lane cameras. Alternatively, clients can customize a daughterboard to suit their requirements.

The daughterboard connector also supports I2C and control signals that enable users to directly interface the camera to the baseboard.

Refer to Section 17.2: [Camera Installation Procedures](#) of the Addendum for installation and operation procedures.

Three numbers of M3 spacers are provided to mount the camera adapter board.

3.7 Audio Interface

The Audio Chip, Part Number [SGTL5000](#) provides audio support on the baseboard. Audio I/O signals are generated through a 2mm header and include the following features:

- Stereo Line-Out
- Mono Mic-In

In addition to the analog audio interface, the dual HDMI 2.0 a/b Video controller supports audio output.

3.8 Serial Ports

Four serial ports are available on the baseboard 2x5 header which are routed from the AGX Xavier Series Module through the programmable [SP336](#) serial transceivers that implement RS232/422/485 protocols via GPIOs.

- Two serial ports configured for RS-232 on the SP336 transceiver are accessible on the 2x5 header.
- Two serial ports are configured with the option to select RS232/422/485 protocol via GPIOs on the SP336 transceiver and are accessible through the 2x5 header.

An on-board Jumper option is provided to select any protocol and terminate RS422 and RS485 protocol transmission lines at 120 Ohm.

NOTE: By default, the Stevie baseboard does not feature a Debug Serial Console Port by default but provides the option to set up a Debug Serial Console by mounting the Jumper at UART-SEL location on **JP2**. This will initiate the Serial Console configuration via serial port 1.

The serial port assignments on the baseboard are specified in the table below.

<i>Port</i>	<i>Connector</i>	<i>Assignment</i>
Port1	J4	ttyTHS0
Port2	J4	ttyTHS1
Port3	J5	ttyTHS4
Port4	J5	ttyTHS6

Refer to Section 17.3: [Serial Multiprotocol Configurations](#) of the Addendum for Multiprotocol Transceiver configuration modes.

3.9 PCIe/USB 3.1/UFS Link Routing Controllers

PCIe Controller

The AGX Xavier Series Module integrate a PCIe 4.0 compliant Root Port controller based on the Synopsys DesignWare PCIe Dual-Mode Controller that supports Gen1, Gen2, Gen3, and Gen4 link speeds up to 16 Gbps. The Dual-Mode Controller supports PCIe endpoint mode operations and incorporates a Direct Memory Access (DMA) Engine to perform DMA data transfer.

USB 2.0/3.0/3.1 Controller

The AGX Xavier Series Module integrates both, an xHCI controller and a USB 3.0 device controller. The xHCI controller supports the xHCI Programming Model for scheduling transactions and interface managements as a Host. The Series Module natively support USB 3.1, USB 2.0, and USB 1.1 transaction functionalities on its USB 3.1 and USB 2.0 interfaces.

The USB 3.0 device controller enables the AGX Xavier Series Module to be accessed from an external Host device. The controller supports USB 2.0 or USB 3.0 with up to 15 IN and 15 OUT Endpoints, which can be configured to support transfer types of different input devices such as a modem or a storage drive.

Both, the xHCI and USB 3.0 device controllers support USB Link Power Management (LPM) features: Remote Wakeup, Wake On Connect, Wake On Disconnect, and Wake On Over Current, in all power states, including Deep Sleep mode.

USB 3.1 ports support both, Gen 1-SuperSpeed and Gen 2-SuperSpeed at 10 Gbps transfer rates. USB 3.1 port 0 and port 3 share one 10 Gbps unit bandwidth, while USB 3.1 is allocated a separate 10 Gbps unit bandwidth. All USB 3.1 ports support hardware initiated U1 and U2 Link Power Management as well as software initiated U3 (suspend) Link Power Management.

Universal Flash Storage (UFS) Controller

The Universal Flash Storage controller in the AGX Xavier Series Module integrates the following blocks:

- A Universal Flash Storage Host Controller (UFSHC)
- A MIPI Unified Protocol (UniPro) Interface Controller
- Two MIPI M-PHY (MPHY) High-Speed Serial Interfaces

The UFS blocks can be operated in single (x1) or dual (x2) lane configurations to support operations at high-speed (HS)-G1, HS-G2, and HS-G3, at both, Rate A and Rate B speeds. MPHY modules drive the physical link and convert parallel data streams from the high-speed serializer into a high-speed differential or low-speed Pulse-Width Modulation (PWM)-like transmissions.

The PCIe, USB 3.1, and UFS Transport Protocol Mapping on the AGX Xavier Series Module is delineated in the table below.

<i>Signal/Pin Name</i>	<i>Mapping</i>
UPHY 0 (x1 PCIe)	Mini PCIe Card
UPHY1 (USB 3.1)	USB 3.1 Header Type A
UPHY [5:2] (x4 PCIe)	M.2 PCIe
UPHY 6 (USB 3.1)	USB 3.1 Header Type A
UPHY 7 (x1 PCIe)	I210 Ethernet Controller
UPHY8 (x1 PCIe)	PCIe to PCI Bridge
UPHY10 (x1 PCIe)	UFS Card Socket

3.10 PCIe MiniCard Socket

The baseboard is equipped with one Mini PCIe socket that supports full-size modules.

Two M2 threaded spacers are mounted on the board for installing a full-size module. A USB 2.0 interface is provided for plugging-in additional cards for expansion and connectivity.

The USB 2.0 port is shared between the USB 2.0 2x5 header at **J19** and the PCIE MiniCard socket.

To connect the USB 2.0 port to the PCIe MiniCard socket, mount the Jumper shunt on **JP2** (USB-SEL) location.

3.11 USB Ports

Stevie baseboard implements four USB 2.0 ports and two USB 3.1 ports. All ports are connected to 1 no. of the 2x5 header.

By default, one USB 2.0 port is routed to the 2x5 header and can be switched to the MiniCard socket using the Jumper option explained in **Section 3.10: PCIe MiniCard Socket** above.

- 2x USB 2.0 port and 2x USB 3.1 ports are connected to Standard Dual USB 3.0 Type A connector.
- 2x USB 2.0 ports are connected to 2x5 header One USB 2.0 port is Muxed between the MiniCard socket and the USB 2.0 socket.

3.12 PCIe M.2 Socket

The baseboard provides a 2280 (22 mm wide and 80 mm long) form factor M.2 PCIe SSD module socket with four PCIe lanes which are routed from the AGX Xavier Series Module. One M2.5 threaded spacers is mounted on the board for installing the 2280 module

Due to physical height constraints of the connector, only single-sided (S2, S3) 2280 M or B+M keyed SSD modules are used on the Stevie baseboard.

3.13 UFS and Micro SD Socket

To enhance interoperability between devices, the baseboard supports a Universal Flash Storage (UFS) Card and MicroSD Card Combo socket with options to insert either or both cards.

3.14 Data Acquisition (DAQ) I/O Interface

The baseboard implements DAQ functionality via:

- Six Single-Ended (SE) Analog-Digital Converter (ADC) inputs or 3 Differential-Ended (DE) inputs
- Two Digital-to-Analog Converter (DAC) outputs
- 13 Digital I/Os through the SAM D51 Microcontroller Series Part No. [ATSAMD51J18A](#)

All ADC, DAC, and Digital I/Os are available on the 2x13 header. The SAM microcontroller interfaces the AGX Xavier Series Module through a Serial Peripheral Interface (SPI) bus.

Refer to Section 14: [Data Acquisition \(DAQ\) Subsystem](#) for more information.

3.15 Controller Area Network (CAN) Interface

The AGX Xavier Series Module integrate two independent CAN ports/channels which support connectivity to two CAN networks. The CAN interfaces are routed to the baseboard via 4-Pin Miniature 1.25mm Pitch latching connectors.

The [TJA1050T](#) CAN Transceiver interfaces between the CAN protocol controller and the physical bus. It enables high-speed applications using baud rates from 60 Kbaud up to 1 Mbaud and provides differential transmission capabilities to the bus and differential receiver capabilities to the CAN protocol controller.

Refer to Section 17.4: [CAN Controller Configuration](#) of the Addendum on configuring the interface.

3.16 Utility Header Connector

The baseboard Power button, Reset, and Force Recovery signals are available through a 2x5 Utility header along with two jumper pins. Optional switches to customize signals are also provided.

3.17 LED Indicators

The baseboard hosts the LED Indicators. The on-board LED Indicator panel is located to the left at the baseboard edge. The LEDs are displayed on a silkscreen panel with a description of their function and status as listed in the table below.

<i>Led Indicators</i>	<i>Description</i>
Power IN	Green LED indicates Power IN
Power ON	Green LED indicates Power Good
Host	Green LED indicates a Successful System Boot
User	Green LED indicates DAQ Controller Chip is ON

4 FUNCTIONAL BLOCK DIAGRAM

4.1 Stevie Baseboard Block Diagram

The following Block Diagram illustrates the key functional blocks of the Stevie baseboard with integrated NVIDIA AGX Xavier Series Module.

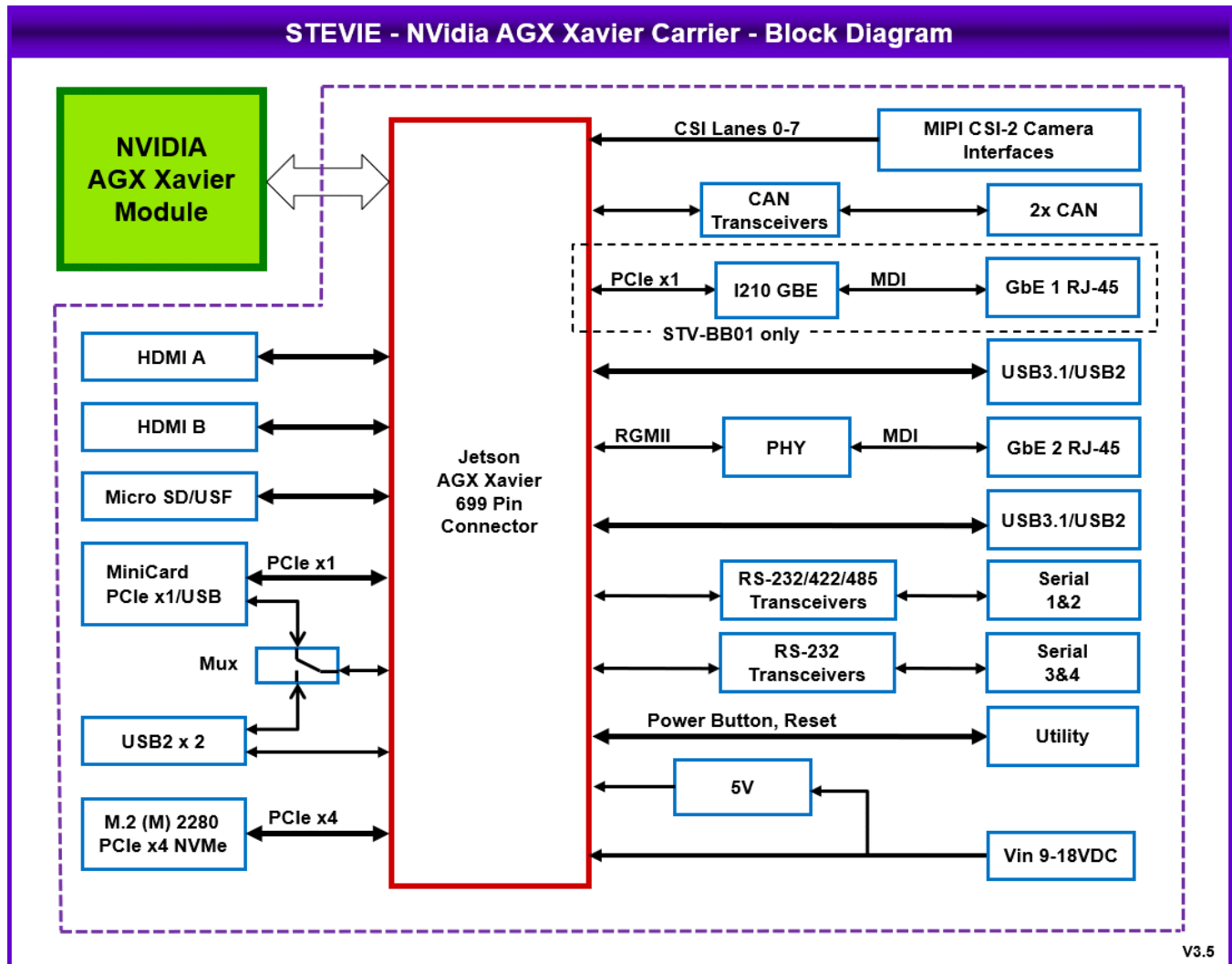


Figure 4-1: Stevie Baseboard Functional Block Diagram

4.2 AGX Xavier Series Module Block Diagram

The following Block Diagram illustrates a high-level view of the AGX Xavier Series components. The ports are broken out through the carrier board.

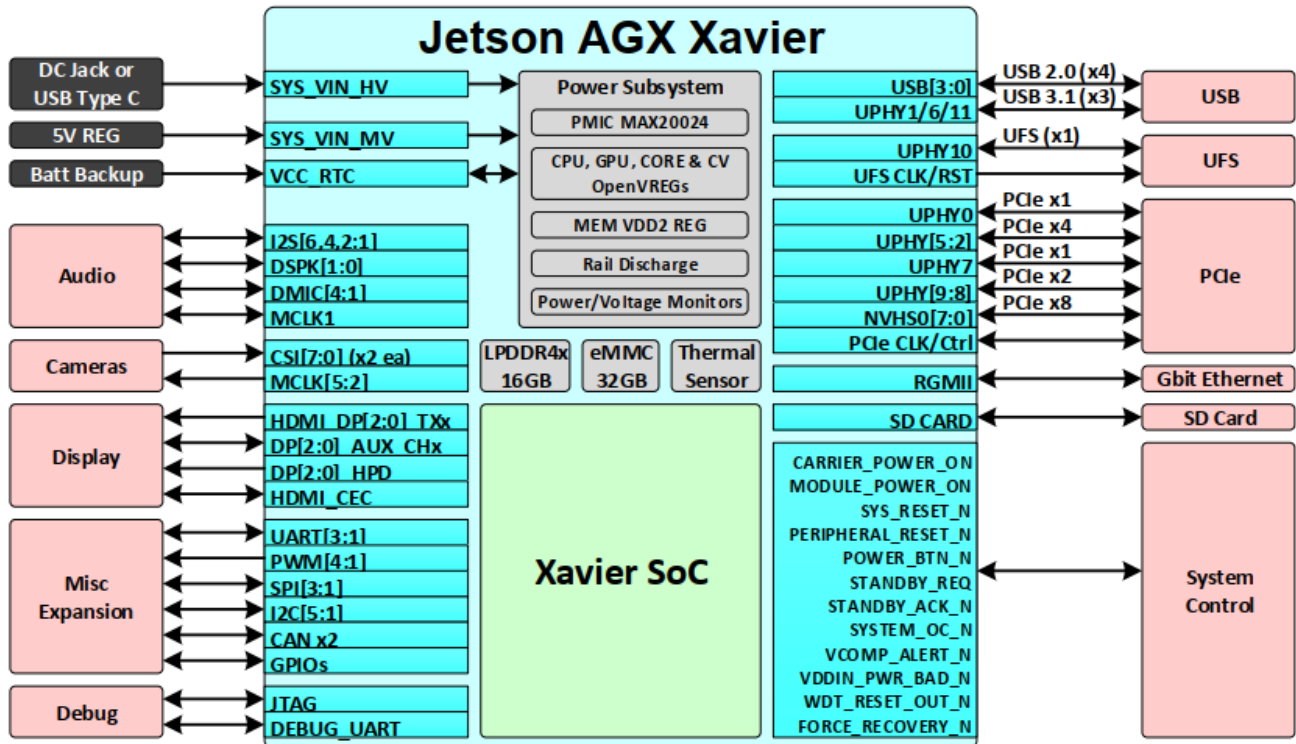


Figure 4-2: AGX Xavier Series Module Functional Block Diagram

5 MECHANICAL DRAWING

Figure 5-1 illustrates the top mechanical view of the Stevie baseboard.

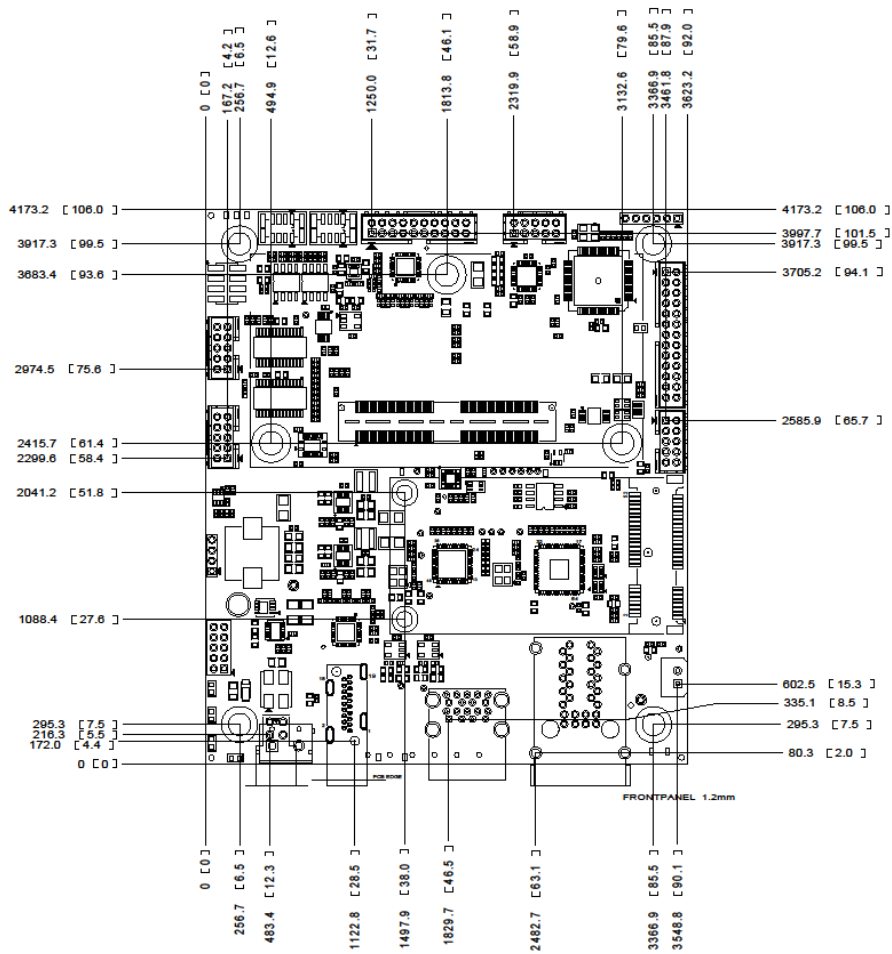


Figure 5-1: Stevie Baseboard Mechanical Top View

6 CONNECTOR AND JUMPER LOCATION

The following figures display the top, bottom and perspective layouts of the Stevie baseboard. A description of the Jumpers and Connectors is tabulated below.

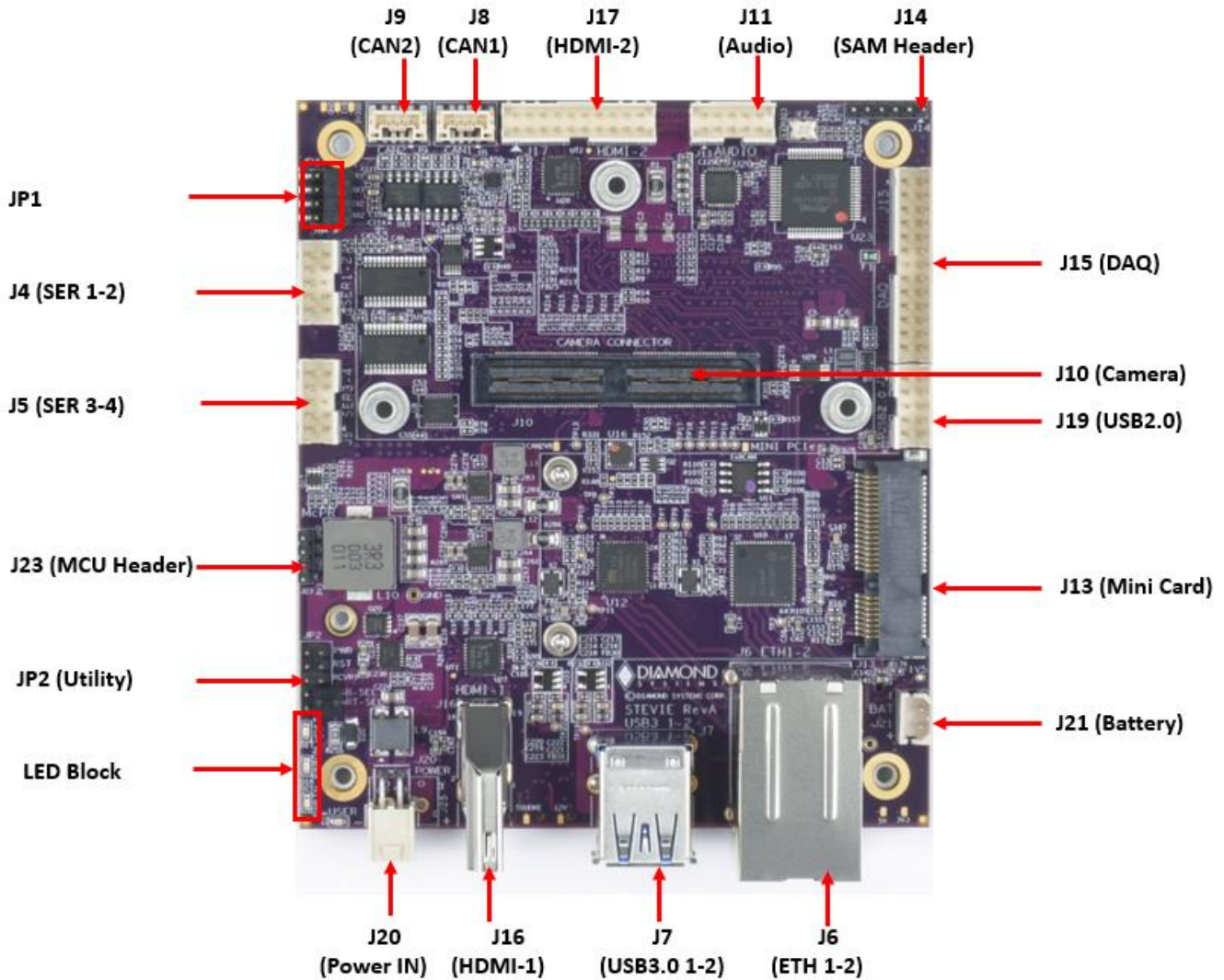


Figure 6-1: Stevie Baseboard Jumper and Connector Layout Top View

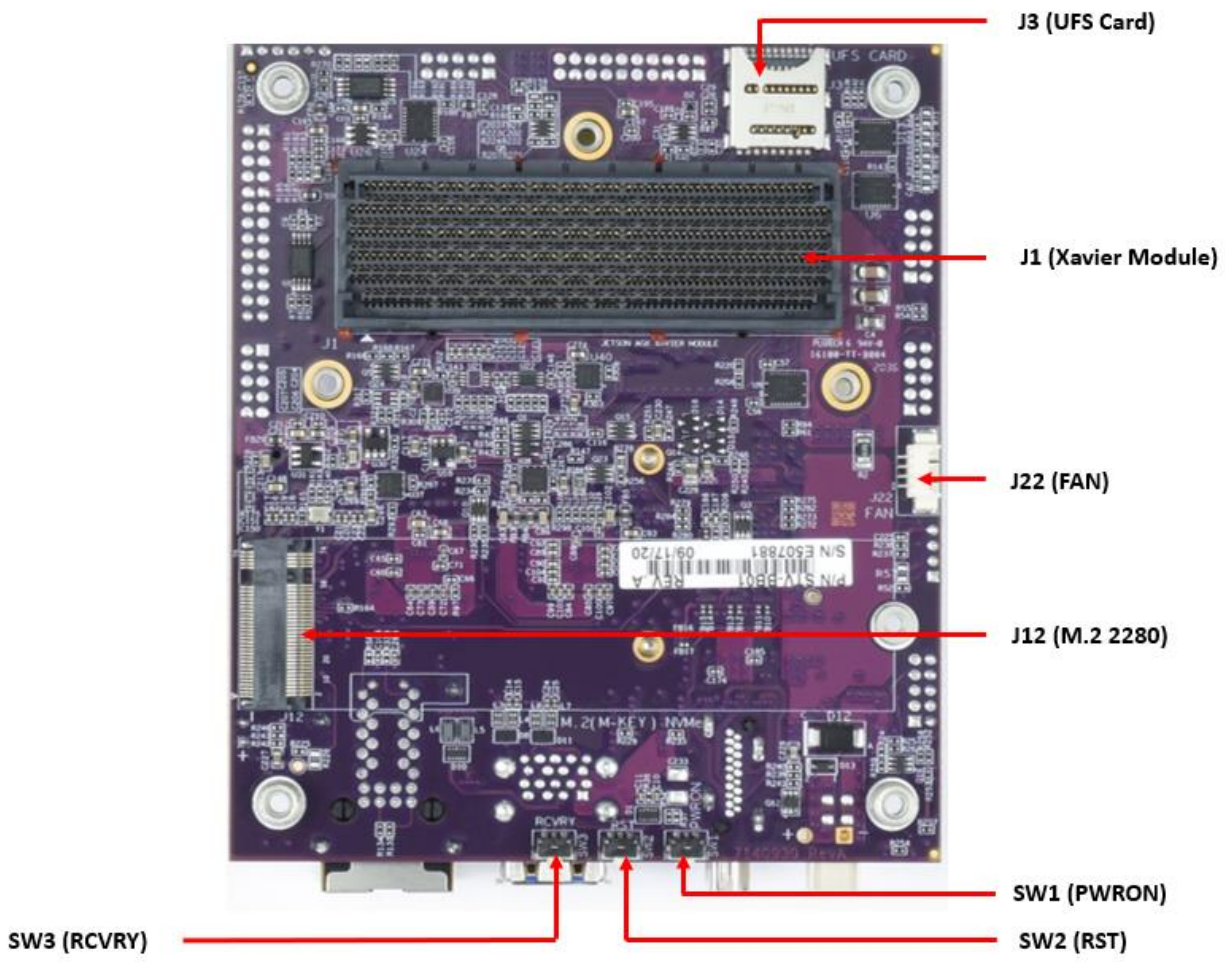


Figure 6-2: Stevie Baseboard Jumper and Connector Layout Bottom View

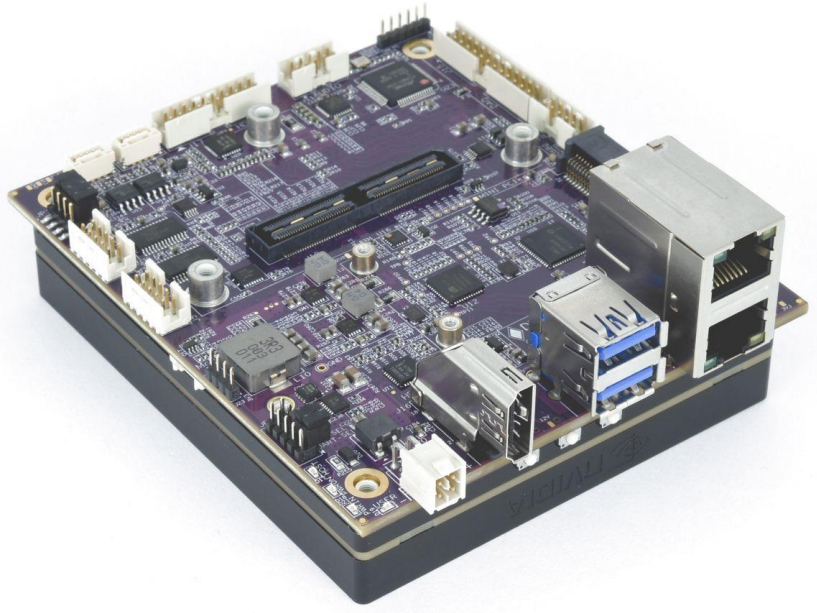


Figure 6-3: Stevie Baseboard with attached AGX Xavier Module Perspective View

7 I/O CONNECTORS, JUMPERS AND LED SPECIFICATIONS

The following table delineates the I/O connectors, Jumpers, and LED Block functions marked in [Figure 6-1](#) and [Figure 6-2](#).

<i>Connector</i>	<i>Function</i>	<i>Jumper</i>	<i>Function</i>
J1 (Bottom)	Xavier Module	JP1	Serial Termination
J2	Utility	JP2	Utility/ Port Selection
J3 (Bottom)	UFS Card		
J4	Serial Headers 1 and 2	LED Block	
J5	Serial Headers 3 and 4	1st LED: Marked in Figure 6-1	Power IN
J6	Ethernet 1 and 2	2nd LED	Power ON
J7	USB 3.0, 1 and 2	3rd LED	HOST LED
J8	CAN 1	4th LED	SAM User LED
J9	CAN 2		
J10	Camera		
J11	Audio		
J12	M.2 PCIe		
J13	Mini PCIe		
J14	SAM/Programming Header		
J15	DAQ		
J16	HDMI-1		
J17	HDMI-2		
J19	USB 2.0		
J20	Power IN		
J21	Battery		
J22 (Bottom)	Fan		
J23	MCU Header		

8 CONNECTOR PINOUT SPECIFICATIONS

8.1 Power IN Connector: J20

+VIN = +9V to +20V

The Power-IN connector supplies power using an input voltage range from +9V to +20V.

NOTE: The AGX Xavier Series Module is not hot-pluggable. Before installing or removing the module, the main power supply pins must be disconnected, and a recommended wait-time of 1-minute must be allowed for the various power rails to fully discharge.

The pinouts for the Power-IN connector are specified below.

VIN	1	2	GND
VIN	3	4	GND

Connector Type: 2x2 Samtec IPL1

Mating Cable Part Number: 6981507

8.2 RTC Battery Connector: J21

RTC BATT = +3.0V

The RTC (Real Time Clock) battery provides power and maintains the internal real-time clock and calendar functions in the system. It serves as an alternate power source when a computer is shut down.

The pinouts for the RTC Battery connector are specified below.

RTC_BATT	1
GND	2

Connector Type: 2x1 Header

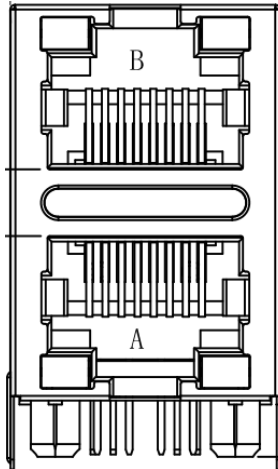
Mating Cable Part Number: 6980524

8.3 Ethernet Connector: J6

The GbE port interface on the baseboard supports a standard dual vertical stacking RJ45 Magjack connector.

The top unit of the receptacle interfaces the I210 port, and the bottom unit interfaces the RGMII port that is connected to the on-board KSZ9031 PHY.

The following illustration depicts the 2-port RJ45 MagJack connector with two USB 3.0 Type-A port pinouts.



Connector Type: 10/100/1000 Base-T, AutoMDIX and two USB 3.0 Type A

Applications: 10/100/1000 Base-T, AutoMDIX

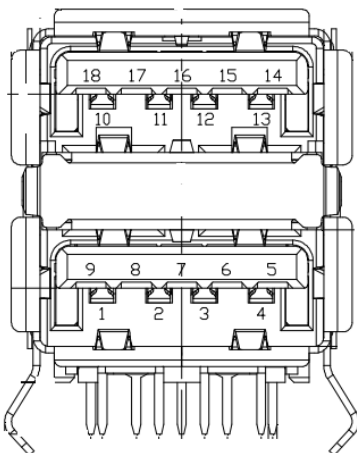
Mounting Type: Through-Hole

Mating Cable Part Number: Standard

8.4 USB 3.0 Ports: J7

The baseboard integrates a standard Stacked USB 3.0/2.0 receptacle.

The following illustration depicts the dual receptacle with two USB 3.0 Type-A port pinouts.



Connector Type: Standard Stacked USB 3.0/2.0 Receptacle; Type A

No. of Positions: 18

Orientation: Right Angle

Mounting Type: Through-Hole

8.5 Audio Connector: J11

The audio signal interface implements audio-port switching functionality with digital microphone & speaker outputs.

Audio signals are terminated at the 2x5 header with the following pinouts.

NOTE: A Line-In feature is not supported by the BSP (Board Support Package).

LineOut-L	A01	B01	LineOut-R
GND_Audio	A02	B02	GND_Audio
LineIn-L	A03	B03	LineIn-R
GND_Audio	A04	B04	GND_Audio
NC	A05	B05	MIC_IN

Connector Type: Standard 2mm Dual-Row Straight Pin Header

Mating Cable Part Number for Latching Connector: 6980608

Mating Cable Part Number for Pin Header: 6981076

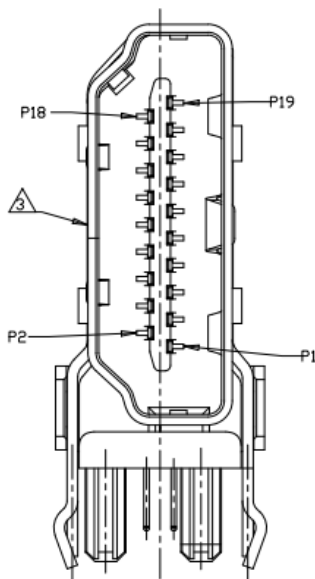
8.6 HDMI Connectors: J16, J17

Stevie baseboard integrates two High-Definition Multimedia Interface (HDMI) receptacle connectors for transmitting uncompressed video data from an HDMI-compliant device, such as a display controller, to a compatible digital screen in video formats and waveforms.

- One HDMI port is routed from the AGX Xavier Series Module and is implemented through the standard HDMI on **J16** Type A connector, which uses a 19-pin configuration to transmit audio and video signals.
- The second HDMI port is routed from the AGX Xavier Series Module and is implemented through the 2x10 header on **J17**.

The connector shell is tied to the chassis Ground.

The following figure illustrates the standard HDMI pinouts.



The pinouts for the **J17** connector are specified below.

Data 2+	A01	B01	Ground
Data 2-	A02	B02	Data 1+
Ground	A03	B03	Data 1-
Data 0+	A04	B04	Ground
Data 0-	A05	B05	Clock+
Ground	A06	B06	Clock-
CEC	A07	B07	Reserved
DDC Clock	A08	B08	DDC Data
Ground	A09	B09	+5V
Hot Plug Detect	A10	B10	Chassis Ground

Connector Type: HDMI Receptacle

Mounting Type: Panel Mount, Through-Hole

Mating Cable Part Number for Latching Connector: 6980605

Mating Cable Part Number for Pin Header: 6980522

8.7 USB 2.0 Connector: J19

The baseboard hosts two USB 2.0 ports

The USB 2.0 interface connector features data and power pins on a pin header. The shield pin is tied to the system ground. The pinouts are specified below.

Key	A01	B01	Shield
USB1 Pwr-	A02	B02	USB0 Pwr-
USB1 Data+	A03	B03	USB0 Data+
USB1 Data-	A04	B04	USB0 Data-
USB1 Pwr+	A05	B05	USB0 Pwr+

Connector Type: Standard 2mm Dual-Row Straight Pin Header

Mating Cable Part Number for Latching Connector: 6980602

Mating Cable Part Number for Pin Header: 6981082

8.8 Camera Expansion Connector: J10

The AGX Xavier Series Module implements a 2x60 expansion socket header for camera installation. The interface includes options for multiple MIPI CSI D-PHY or C-PHY interfaces for cameras, an 8-lane SLVS camera interface and audio signals.

The 4x4 CSI lanes from the AGX Xavier Series Module terminate at the 60x2 header.

The pinouts are specified below.

CSI_0_D0_P	1	2	CSI_1_D0_P	CSI_5_CLK_P	65	66	CSI_7_CLK_P
CSI_0_D0_N	3	4	CSI_1_D0_N	CSI_5_CLK_N	67	68	CSI_7_CLK_N
GND	5	6	GND	GND	69	70	GND
CSI_0_CLK_P	7	8	CSI_1_CLK_P	CSI_5_D1_P	71	72	CSI_7_D1_P
CSI_0_CLK_N	9	10	CSI_1_CLK_N	CSI_5_D1_N	73	74	CSI_7_D1_N
GND	11	12	GND	I2C_GP3_CLK	75	76	SNN_CAM_76
CSI_0_D1_P	13	14	CSI_1_D1_P	I2C_GP3_DAT	77	78	SNN_CAM_HSYNC
CSI_0_D1_N	15	16	CSI_1_D1_N	GND	79	80	GND
GND	17	18	GND	AVDD_CAM_2V8	81	82	AVDD_CAM_2V8
CSI_2_D0_P	19	20	CSI_3_D0_P	AVDD_CAM_2V8	83	84	VDD_AF
CSI_2_D0_N	21	22	CSI_3_D0_N	CAM_AF_PWDN	85	86	SNN_CAM_VSYNC
GND	23	24	GND	I2C_GP2_CLK	87	88	CAM1_MCLK03
CSI_2_CLK_P	25	26	CSI_3_CLK_P	I2C_GP2_DAT	89	90	GPIO15_CAM1_PWDN
CSI_2_CLK_N	27	28	CSI_3_CLK_N	CAM0_MCLK02	91	92	GPIO16_CAM1_RST
GND	29	30	GND	CAM0_PWDN	93	94	CAM2_MCLK04
CSI_2_D1_P	31	32	CSI_3_D1_P	CAM0_RST_BUFFER	95	96	SNN_CAM2_PWDN
CSI_2_D1_N	33	34	CSI_3_D1_N	SNN_FLASH_EN	97	98	SNN_CAM2_RST
GND	35	36	GND	GND	99	100	GND
CSI_4_D0_P	37	38	CSI_6_D0_P	DVDD_CAM_IO	101	102	VDD_1V8
CSI_4_D0_N	39	40	CSI_6_D0_N	SNN_FLASH_MASK	103	104	SNN_TORCH_EN
GND	41	42	GND	I2C_GP4_CLK	105	106	SNN_FLASH_STROBE
CSI_4_CLK_P	43	44	CSI_6_CLK_P	I2C_GP4_DAT	107	108	VDD_3V3
CSI_4_CLK_N	45	46	CSI_6_CLK_N	VDD_IR	109	110	VDD_3V3
GND	47	48	GND	SNN_SPI_SCK	111	112	SNN_SPI_DIN
CSI_4_D1_P	49	50	CSI_6_D1_P	SNN_SPI_CS0	113	114	SNN_SPI_DOUT
CSI_4_D1_N	51	52	CSI_6_D1_N	GND	115	116	GND
GND	53	54	GND	CAM_INTR	117	118	VDD_3V3
DVDD_CAM_LV	55	56	DVDD_CAM_LV	GPIO25_VDD_SYS_EN	119	120	VDD_3V3
DVDD_CAM_LV	57	58	DVDD_CAM_LV	GND	121	122	GND
CSI_5_D0_P	59	60	CSI_7_D0_P	GND	123	124	GND
CSI_5_D0_N	61	62	CSI_7_D0_N	GND	125	126	GND
GND	63	64	GND	GND	127	128	GND

Connector Number: Samtec QSH-060-01-H-D-A-K-TR

Mating Connector Part Number: Samtec QTH-060-01-L-D-A

Manufacturer: e-Con Systems, Leopard Imaging

8.9 Serial Port Connectors: J4, J5

The AGX Xavier Series Module supports four serial ports available at two headers. Each connector supports 2 serial ports.

The pinouts specific to the transceiver interfaces RS232/ RS422/ RS485 are as follows.

RS-232 Interface

TX1	A01	B01	RTS1
RX1	A02	B02	CTS1
GND	A03	B03	GND
TX2	A04	B04	RTS2
RX2	A05	B05	CTS2

RS-422 Interface

TX1+	A01	B01	TX1-
RX1 +	A02	B02	RX1-
GND	A03	B03	GND
TX2+	A04	B04	TX2-
RX2+	A05	B05	RX2-

RS-485 Interface

TX1/RX1+	A01	B01	TX1/RX1-
NC	A02	B02	NC
GND	A03	B03	GND
TX2/RX2+	A04	B04	TX2/RX2-
NC	A05	B05	NC

Connector Type: Standard 2mm Dual-Row Straight Pin Header with Gold Flash Plating

Mating Connector Part Number for Latching Connector: 6980601

Mating Cable Part Number for Pin Header: 6981075

8.10 Fan Connector: J22

Fan connector pinouts are defined as below. Customer can make Fan cable based on the Fan selected.

PWM (5V)	1
Tach In (1.8V OD)	2
5V	3
Ground	4

Connector Type: 1.25mm Single Row SMD RA

Housing Part Number: 0510210400

8.11 PCIe MiniCard Connector: J13

The TX (Transmit) and RX (Receive) signals are transmitted by the host.

The TX signal channels on the socket and the RX signal channels on the AGX Xavier Series Module are bi-directional. The RX signal on the socket is driven by the TX signal on the installed module and vice versa. The Chip Select (CS) control feature is available to generate commands on the SPI bus.

The two mounting standoffs at the far end of the AGX Xavier Series Module installation site are not connected to Ground.

The pinouts are specified below.

	1	2	+3.3V
	3	4	Gnd
	5	6	+1.5V
Clkreq-	7	8	
Gnd	9	10	
PCIe 1 Clk-	11	12	
PCIe 1 Clk+	13	14	
Gnd	15	16	
KEY			
	17	18	Gnd
	19	20	Disable-
Gnd	21	22	PCIe Reset-
PCIe 1 RX-	23	24	+3.3V
PCIe 1 RX+	25	26	Gnd
Gnd	27	28	+1.5V
Gnd	29	30	SMB Clk
PCIe 1 TX-	31	32	SMB Data
PCIe 1 TX+	33	34	Gnd
Gnd	35	36	USB2-
Gnd	37	38	USB2+
+3.3V	39	40	Gnd
+3.3V	41	42	WWAN LED-
Ground	43	44	WLAN LED-
	45	46	WPAN LED-
	47	48	+1.5V
Pull-up to +3.3V	49	50	Gnd
	51	52	+3.3V

Connector Part Number: MM60-52B1-E1-R650

8.12 M.2 PCIe SSD Socket (M-KEY) Connector: J12

Stevie baseboard is equipped with an M-keyed connector.

An M.2 SSD is "keyed" to prevent the insertion of a card connector to an incompatible socket on the host. There are three keys that are commonly used: B, M, and B+M with the key type is typically labeled on or near the edge of the gold-plated fingers on the connector of the SSD.

One mounting standoff at the far end of the module installation site is not connected to Ground.

The pinouts are specified below.

GND	1	2	3.3V
GND	3	4	3.3V
PETn3	5	6	N/C
PETp3	7	8	N/C
GND	9	10	LED1#
PERn3	11	12	3.3V
PERp3	13	14	3.3V
GND	15	16	3.3V
PETn2	17	18	3.3V
PETp2	19	20	N/C
GND	21	22	N/C
PERn2	23	24	N/C
PERp2	25	26	N/C
GND	27	28	N/C
PETn1	29	30	N/C
PETp1	31	32	N/C
GND	33	34	N/C
PERn1	35	36	N/C
PERp1	37	38	N/C
GND	39	40	N/C
PETn0	41	42	N/C
PETp0	43	44	N/C
GND	45	46	N/C
PERn0	47	48	N/C
PERp0	49	50	PERST#
GND	51	52	CLKREQ#
REFCLKN	53	54	PEWake#
REFCLKP	55	56	N/C
GND	57	58	N/C
KEY			
N/C	67	68	SUSCLK
PEDET	69	70	3.3V
GND	71	72	3.3V
GND	73	74	3.3V
GND	75		

Connector Part Number: MDT320M03001

8.13 Data Acquisition (DAQ) Connector: J15

The baseboard implements a multifunction Digital I/O circuit that integrates analog input and output, digital input and output, and counter/timer functionalities.

The pinouts specified below.

AIN0 / 0-	A01	B01	AIN1 / 0+
AIN2 / 1-	A02	B02	AIN3 / 1+
AIN4 / 2-	A03	B03	AIN5 / 2+
DAC0	A04	B04	DAC1
Aground	A05	B05	Aground
Dground	A06	B06	+3.3V Fused
DIO 0	A07	B07	DIO 1
DIO 2	A08	B08	DIO 3
DIO 4	A09	B09	DIO 5
DIO 6	A10	B10	DIO 7
DIO 8	A11	B11	DIO 9
DIO 10	A12	B12	DIO11
DIO 12 /RESET_IN	A13	B13	Dground

The following table provides the signal type and its definition.

<i>Signal Name</i>	<i>Definition</i>
AIN 5-0/AIN 2-0	Single/Differential Ended Analog Inputs at 3.3V Level
DAC 1-0	DAC Outputs at 3.3V Level
DIO 11-0	Digital I/O Port. Programmable Direction at 3.3V Level
DIO 12/RESET_IN	Digital IO at 3.3V Level. Reset in Signal at 1.8V Level
Dground	Digital Ground
Aground	Analog Ground

Connector Type: Standard 2mm Dual-Row Straight Pin Header

Mating Connector Part Number for Latching Connector: 6980606

Mating Cable Part Number for Pin Header: 6980516

8.14 Utility Connector: JP2

The following table provides the pinouts for the utility connector.

UART_SEL	1	2	Ground
USB-SEL	3	4	Ground
Force Recovery	5	6	Ground
Reset In	7	8	Ground
Power Button	9	10	Ground

Connector Type: Standard 2mm Dual-Row Straight Pin Header

Cable Part Number: TBD

8.15 CAN Connectors: J8, J9

There are two identical on-board CAN interface connectors that are routed from the AGX Xavier Series Module. The pinouts are derived from DS-MPE-CAN2L and are specified below.

Ground	1
CAN Low	2
CAN High	3
Ground	4

Connector Type: 1.25mm Single Row SMD RA

Cable Part Number: 6981182

8.16 UFS Interface Connector: J3

The AGX Xavier Series Module supports a x1 lane UFS interface.

The pinouts for the connector are specified below.

1	VSS
2	DIN_C
3	DIN_T
4	VSS
5	DOUT_C
6	DOUT_T
7	VSS
8	REFCLK
9	VCCQ2
10	GND
11	VSS
12	VCC
13	DATA1
14	DATA0
15	CLK
16	CMD
17	DATA3
18	DATA2
19	C_DETECT
20	GND
21	GND
22	GND
23	GND
24	GND
25	GND

Connector Type: Standard UFS + Micro SD Connector

Manufacturer: Amphenol

8.17 Jetson Xavier B2B Connector Interface (J1)

The following table figure depicts Jetson AGX Xavier Series Module Connector Pin Out Matrix Part 1: Columns A – F.

	A	B	C	D	E	F
01			SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV
02			SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV
03	PRSVT0	SYS_VIN_HV	GND	SYS_VIN_HV	GND	SYS_VIN_HV
04	SDCARD_D2	GND	RGMII_RD0	GND	I2S2_FS	GND
05	SDCARD_CMD	RGMII_TXC	RGMII_RXC	RGMII_RX_CTL	RGMII_RD3	I2S2_DOUT
06	UFS0_REF_CLK	SDCARD_CLK	UFS0_RST_N	SDCARD_D3	RGMII_SMA_MDC	I2S2_DIN
07	GPIO9	GND	I2S1_SDCOUT	GND	RGMII_SMA_MDIO	GND
08	PEX_WAKE_N	GPIO11	PEX_L5_CLKREQ_N	I2S1_FS	SDCARD_D0	SDCARD_D1
09	GND	PEX_L1_RST_N	GND	PEX_L1_CLKREQ_N	GND	GPIO16
10	USB2_P	RSVD	USB1_N	PEX_LD_RST_N	GPIO12	GPIO15
11	USB2_N	GND	USB1_P	GND	PEX_LD_CLKREQ_N	GND
12	GND	UPHY_RX10_P	GND	UPHY_RX11_P	GND	USB0_P
13	GND	UPHY_RX10_N	GND	UPHY_RX11_N	GND	USB0_N
14	UPHY_RX8_N	GND	UPHY_RX9_N	GND	PEX_CLK0_N	GND
15	UPHY_RX8_P	GND	UPHY_RX9_P	GND	PEX_CLK0_P	GND
16	GND	UPHY_RX6_P	GND	UPHY_RX7_P	GND	PEX_CLK1_P
17	GND	UPHY_RX6_N	GND	UPHY_RX7_N	GND	PEX_CLK1_N
18	UPHY_RX4_P	GND	UPHY_RX5_N	GND	RSVD	GND
19	UPHY_RX4_N	GND	UPHY_RX5_P	GND	RSVD	GND
20	GND	UPHY_RX2_N	GND	UPHY_RX3_P	GND	PEX_CLK3_P
21	GND	UPHY_RX2_P	GND	UPHY_RX3_N	GND	PEX_CLK3_N
22	UPHY_RX0_P	GND	UPHY_RX1_N	GND	PEX_CLK4_N	GND
23	UPHY_RX0_N	GND	UPHY_RX1_P	GND	PEX_CLK4_P	GND
24	GND	NVHS0_SLVS_RX1_N	GND	NVHS0_SLVS_RX0_P	GND	PEX_CLK5_P
25	GND	NVHS0_SLVS_RX1_P	GND	NVHS0_SLVS_RX0_N	GND	PEX_CLK5_N
26	NVHS0_SLVS_RX3_P	GND	NVHS0_SLVS_RX2_N	GND	UPHY_REFCLK1_N	GND
27	NVHS0_SLVS_RX3_N	GND	NVHS0_SLVS_RX2_P	GND	UPHY_REFCLK1_P	GND
28	GND	NVHS0_SLVS_RX5_N	GND	NVHS0_SLVS_RX4_P	GND	RSVD
29	GND	NVHS0_SLVS_RX5_P	GND	NVHS0_SLVS_RX4_N	GND	RSVD
30	NVHS0_SLVS_RX7_P	GND	NVHS0_SLVS_RX6_N	GND	NVHS0_SLVS_REFCLK0_P	GND
31	NVHS0_SLVS_RX7_N	GND	NVHS0_SLVS_RX6_P	GND	NVHS0_SLVS_REFCLK0_N	GND
32	GND	RSVD	GND	RSVD	GND	RSVD
33	GND	RSVD	GND	RSVD	GND	RSVD
34	RSVD	GND	RSVD	GND	RSVD	GND
35	RSVD	GND	RSVD	GND	RSVD	GND
36	GND	RSVD	GND	RSVD	GND	RSVD
37	GND	RSVD	GND	RSVD	GND	RSVD
38	RSVD	GND	RSVD	GND	CSI0_D1_N	GND
39	RSVD	GND	RSVD	GND	CSI0_D1_P	GND
40	GND	MID4	GND	MID3	GND	MID2
41	CSI2_D0_P	GND	CSI2_D1_N	GND	CSI0_D0_N	GND
42	CSI2_D0_N	CSI2_CLK_N	CSI2_D1_P	CSI5_D0_P	CSI0_D0_P	CSI0_CLK_N
43	GND	CSI2_CLK_P	GND	CSI5_D0_N	GND	CSI0_CLK_P
44	CSI7_D0_P	GND	CSI5_CLK_P	GND	CSI3_D0_N	GND
45	CSI7_D0_N	CSI7_CLK_P	CSI5_CLK_N	CSI5_D1_N	CSI3_D0_P	CSI3_CLK_N
46	GND	CSI7_CLK_N	GND	CSI5_D1_P	GND	CSI3_CLK_P
47	HDMI_DP1_TX0_P	GND	CSI7_D1_P	GND	CSI4_D1_P	GND
48	HDMI_DP1_TX0_N	HDMI_DP1_TX1_N	CSI7_D1_N	HDMI_DP1_TX2_N	CSI4_D1_N	CSI4_CLK_P
49	GND	HDMI_DP1_TX1_P	GND	HDMI_DP1_TX2_P	GND	CSI4_CLK_N
50	HDMI_DP2_TX2_N	GND	HDMI_DP2_TX3_N	GND	HDMI_DP1_TX3_P	GND
51	HDMI_DP2_TX2_P	HDMI_DP2_TX1_P	HDMI_DP2_TX3_P	HDMI_DP2_TX0_P	HDMI_DP1_TX3_N	DP0_AUX_CH_N
52	GND	HDMI_DP2_TX1_N	GND	HDMI_DP2_TX0_N	GND	DP0_AUX_CH_P
53	I2C5_CLK	GND	I2C5_DAT	GND	I2C3_DAT	I2C3_CLK
54	GPIO17	WDT_RESET_OUT_N	GPIO33	GPIO03	FAN_TACH	GPIO22
55	GPIO34	GPIO30	GPIO18	SPI1_MOSI	SPI1_CS0_N	SPI3_CLK
56	SPI1_MISO	SPI1_CS1_N	UART2_RX	SPI3_MISO	SPI3_CS1_N	GPIO36
57	UART2_CTS	GND	SPI3_CS0_N	GND	GND	GND
58	GPIO20	GPIO21	UART2_TX	JTAG_TDO	JTAG_TMS	CAN0_DIN
59	GPIO05	GPIO04	I2S3_SCLK	CAN0_DOUT	GPIO06	GPIO07
60	JTAG_TCK	JTAG_TDI	I2S3_FS	SPI2_CS0_N	I2C4_DAT	SPI2_MOSI
61	SYSTEM_OC_N	CAN1_DIN	GPIO09	I2C4_CLK	SPI2_CLK	VCOMP_ALERT_N
62	GPIO10	GPIO08	GND	SPI2_MISO	GND	GND
63	GND	SYS_VIN_HV	SYS_VIN_HV	GND	SYS_VIN_HV	SYS_VIN_HV
64			SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV
65			SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV

Legend Ground Power Reserved—Must be left unconnected unless otherwise directed.

The following table figure depicts Jetson AGX Xavier Series Module Connector Pin Out Matrix Part 2: Columns G – L.

	G	H	J	K	L
01	SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV		
02	SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV		
03	GND	SYS_VIN_HV	GND	SYS_VIN_HV	GND
04	I2S2_CLK	GND	GPIO01	GND	UART4_RTS
05	RGMII_TD1	ENET_RST_N	ENET_INT	I2C1_CLK	UART4_TX
06	RGMII_TD3	RGMII_RD2	RGMII_TD0	RGMII_RD1	GPIO02
07	GPIO13	GND	RGMII_TD2	RGMII_TX_CTL	GND
08	PEX_L4_CLKREQ_N	I2S1_SDIN	GND	GND	I2C1_DAT
09	GND	MCLK01	PEX_L4_RST_N	PEX_L3_RST_N	GPIO28
10	USB3_N	PEX_L5_RST_N	PEX_L3_CLKREQ_N	RSVD	FORCE_RECOVERY_N
11	USB3_P	GND	RSVD	GND	STANDBY_REQ_N
12	GND	UPHY_TX11_P	GND	UPHY_TX10_N	GND
13	GND	UPHY_TX11_N	GND	UPHY_TX10_P	GND
14	UPHY_TX9_N	GND	UPHY_TX8_P	GND	I2S1_CLK
15	UPHY_TX9_P	GND	UPHY_TX8_N	GND	GPIO14
16	GND	UPHY_TX7_P	GND	UPHY_TX6_N	GND
17	GND	UPHY_TX7_N	GND	UPHY_TX6_P	GND
18	UPHY_TX5_N	GND	UPHY_TX4_P	GND	RSVD
19	UPHY_TX5_P	GND	UPHY_TX4_N	GND	RSVD
20	GND	UPHY_TX3_P	GND	UPHY_TX2_N	GND
21	GND	UPHY_TX3_N	GND	UPHY_TX2_P	GND
22	UPHY_TX1_N	GND	UPHY_TX0_P	GND	SYS_VIN_MV
23	UPHY_TX1_P	GND	UPHY_TX0_N	GND	SYS_VIN_MV
24	GND	NVHS0_TX0_P	GND	NVHS0_TX1_N	GND
25	GND	NVHS0_TX0_N	GND	NVHS0_TX1_P	GND
26	NVHS0_TX2_N	GND	NVHS0_TX3_P	GND	SYS_VIN_MV
27	NVHS0_TX2_P	GND	NVHS0_TX3_N	GND	SYS_VIN_MV
28	GND	NVHS0_TX4_P	GND	NVHS0_TX5_N	GND
29	GND	NVHS0_TX4_N	GND	NVHS0_TX5_P	GND
30	NVHS0_TX6_N	GND	NVHS0_TX7_P	GND	SYS_VIN_MV
31	NVHS0_TX6_P	GND	NVHS0_TX7_N	GND	SYS_VIN_MV
32	GND	RSVD	GND	RSVD	GND
33	GND	RSVD	GND	RSVD	GND
34	RSVD	GND	RSVD	GND	SYS_VIN_MV
35	RSVD	GND	RSVD	GND	SYS_VIN_MV
36	GND	RSVD	GND	RSVD	GND
37	GND	RSVD	GND	RSVD	GND
38	RSVD	GND	RSVD	GND	SYS_VIN_MV
39	RSVD	GND	RSVD	GND	SYS_VIN_MV
40	GND	MID1	GND	MID0	GND
41	CSI1_D0_P	GND	CSI1_D1_P	GND	VM_EN1_N
42	CSI1_D0_N	CSI1_CLK_N	CSI1_D1_N	GND	VM_EN0_N
43	GND	CSI1_CLK_P	GND	CSI6_D0_N	GND
44	CSI3_D1_P	GND	CSI6_CLK_P	CSI6_D0_P	VM_I2C_SCK
45	CSI3_D1_N	CSI6_D1_N	CSI6_CLK_N	GND	VM_I2C_DAT
46	GND	CSI6_D1_P	GND	HDMI_DP0_TX3_P	GND
47	CSI4_D0_N	GND	HDMI_DP0_TX2_P	HDMI_DP0_TX3_N	VM_INT_N
48	CSI4_D0_P	HDMI_DP0_TX0_N	HDMI_DP0_TX2_N	GND	UART4_RX
49	GND	HDMI_DP0_TX0_P	GND	GPIO25	UART4_CTS
50	HDMI_DP0_TX1_N	GND	HDMI_CEC	DP2_HPD	GPIO35
51	HDMI_DP0_TX1_P	GPIO26	GPIO24	DP1_HPD	UART_RTS
52	GND	GPIO27	DP1_AUX_CH_P	DP0_HPD	OVERTEMP_N
53	DP2_AUX_CH_P	MCLK03	DP1_AUX_CH_N	UART1_TX	VCC_RTC
54	DP2_AUX_CH_N	UART1_CTS	MCLK02	UART1_RX	MODULE_POWER_ON
55	GPIO23	MCLK04	GPIO32	GND	VDDIN_PWR_BAD_N
56	SPI3_MOSI	GND	GND	GPIO19	TEMP_ALERT_N
57	GND	UART5_CTS	SPI1_CLK	PWM01	MCLK05
58	UART2_RTS	UART5_RX	UART5_TX	UART5_RTS	PERIPHERAL_RESET_N
59	NC_03	NVJTAG_SEL	I2S3_DIN	I2S3_DOUT	SAFETY_PROCESSOR_GPIO
60	NVDBG_SEL	GPIO31	STANDBY_ACK_N	UART3_RX_DEBUG	SYS_RESET_N
61	JTAG_TRST_N	CAN1_DOUT	I2C2_CLK	I2C2_DAT	POWER_BTN_N
62	GND	UART3_TX_DEBUG	GND	FAN_PWM	CARRIER_POWER_ON
63	SYS_VIN_HV	GND	SYS_VIN_HV	GND	PRSNT1
64	SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV		
65	SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV		

Legend	Ground	Power	Reserved - See UART1 section for UART4_RX handling in the OEM PRODUCT DESIGN GUIDE, NVIDIA Jetson AGX Xavier Series
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9 I/O CONNECTOR LIST

The following table provides a summary of the I/O connectors on the Stevie baseboard.

<i>Function</i>	<i>Manufacturer</i>	<i>Part No.</i>	<i>Description</i>	<i>DSC Mating Cable</i>
Power IN	Samtec	IPL1-102-01-D-RA-K	2x2 Box Header T/H Right Angle .1" Pitch	6981507
External Battery	Molex	22-03-5025	2 Pos. TH VERT HDR, 2.5 MM Shrouded	6980524
GbE Ethernet and USB 3.1 (x2)	GbE Ethernet	LPJU3724BHNL	RJ45 Combo and USB 3.0 Dual	N/A
HDMI 1	TE	2007435-1	HDMI RCPT TYPE A R/A TH	N/A
HDMI 2	FCI	98414-F06-20ULF	2x10, 2 mm Pitch, TH Header	6980605
Camera (x4)	Samtec	QSH-060-01-H-D-A-K-TR	2x60 0.5 mm Pitch	NA
Serial Ports (x4)	FCI	98414-G06-10LF	2x5, 2 mm Pitch, TH Header	6980601
Audio	FCI	98414-G06-10LF	2x5, 2 mm Pitch, TH Header	6980608
USB 2.0	FCI	98414-G06-10LF	2x5, 2 mm Pitch, TH Header	6980602
CAN (x2)	JST	BM04B-GHS-TBT	1x4, 1.25 mm Pitch, SMT	6981182
DAQ	FCI	98414-G06-26ULF	2x13, 2 mm Pitch, TH Header	6980606
Utility	PINREX	220-9205GB01	2x5, 2 mm Pitch, TH Header	N/A
Fan	Molex	0532610471s	1x4, 1.25 mm Pitch, SMT RA	N/A
PCIe MiniCard	JAE	MM60-52B1-E1-R650	52-Pin MiniCard, Full Size, with PCB Mount Threaded Spacers	N/A
M.2 SSD Socket	Amphenol	MDT320M03001	75-pin M.2 M Keyed Socket, 2242 with PCB Mount Threaded Spacer	N/A
UFS	Amphenol	1010170469 #2A	CONN UFS and Micro SD Push-Pull	N/A
Module Connector	Molex	2034560003	699-Pin Board-to-Board Connector/B2B, 8 mm	N/A

9.1 I/O Cables

CK-STEVEIE-01 Package

CK-STEVEIE-01 Non-Latching Cables are industry-standard cables that are required during installation. The following table provides Non-Latching Cable specifications included in the CK-STEVEIE-01 package.

<i>Photo No</i>	<i>Cable Part No.</i>	<i>Description</i>	<i>Stevie Connector</i>
1	6981507	Power Cable	J20
2	6980524	External Battery	J21
3	6980601	Serial Ports	J4, J5
4	6980602	USB 2.0 TYPE A Panel Mount	J19
7	6980605	HDMI Cable	J17
8	6980606	DAQ Cable	J15
9	6980608	Audio Cable	J11
10	6981182	CAN Bus 2.0 Cable	J8, J9

10 JUMPER DESCRIPTION

The Jumper blocks on the baseboard can be configured to enable/disable or alter the default signal routing settings on the circuit, using Jumper shunts.

The following table describes the Jumper Blocks on the baseboard. Refer to [Figure 6-1](#) for Jumper Locations.

<i>Jumper</i>	<i>Description</i>
JP1	Serial Termination
JP2	Debug port/Minicard Selection

10.1 Serial Termination Selection (JP1)

The **JP1** block settings can be switched to operate in different modes. The mode is selected using Jumper shunts.

Termination resistors for RS422/RS485 modes can be set using Jumpers on pin headers for serial ports 1 and 2.

The following table shows the positions, function, and termination modes on the **JP1** block. The text in bold and italics mark the default configuration on **JP1**.

<i>Position</i>	<i>Function</i>	<i>IN</i>	<i>OUT</i>
TX1	Serial Port1 TX Termination	Enabled	<i>Disabled</i>
RX1	Serial Port1 RX Termination	Enabled	<i>Disabled</i>
TX2	Serial Port2 TX Termination	Enabled	<i>Disabled</i>
RX2	Serial Port2 RX Termination	Enabled	<i>Disabled</i>

The following figure illustrates the default Jumper settings on the **JP1** block.



Figure 10-1: Jumper JP1 Default Locations

10.2 Debug UART& MiniCard USB Selection (JP2)

Access to UART serial console port on Serial port1 on J4 connector can be selected using .this jumper.

One if the USB2.0 port is shared between minicard (J13) and USB2.0 header (J19). By default, it is connected to USB2.0 header (J19). USB2.0 port to minicard can be enabled using this JP2 jumper.

The following table shows the pinout, function, and attributes for the **JP2** block. The text in bold and italics mark the default configuration.

<i>Position</i>	<i>Function</i>	<i>IN</i>	<i>OUT</i>
UART-SEL	Debug UART	Enabled	<i>Disabled</i>
USB-SEL	USB2.0 SEL	MiniCard	<i>2 x 5 Header</i>

The following figure illustrates the default Jumper settings on the **JP2** block. Other 3 location are used for utility signals.

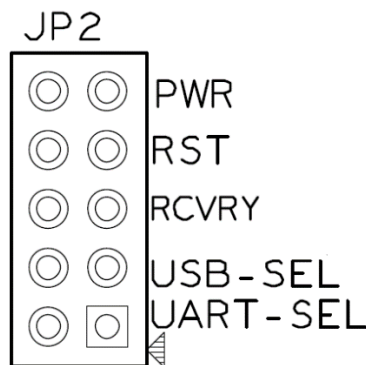


Figure 10-2: Jumper JP2 Default Locations

11 GETTING STARTED

This section covers the following topics.

- Jetson AGX Xavier Module Installation and Removal
- Information about the required components essential to install the hardware to flash the baseboard.
- Instructions to configure and setup the baseboard.
- Instructions to verify and confirm the installation process completed successfully.

11.1 Jetson AGX Xavier Module Installation and Removal

This section is applicable if the AGX Xavier module is not already installed on the Stevie baseboard.

To install the Jetson AGX Xavier Series module correctly, follow the following sequence and mounting hardware instructions.

1. Connectors should be parallel with respect to each other during mating.
2. Use a smooth motion during mating (no mechanical shock, knocking, hammering).
3. Secure with M3 screws (4x) from top of the module. Torque the screws to 2.5 lbf-in.

To remove the Jetson AGX Xavier Series module correctly, follow the following sequence and mounting hardware instructions.

1. Remove mounting screws M3 screws (4x) from top of the module.
2. Rock the Stevie board a few times, no more than ± 3 degrees, to gradually disengage the connectors.

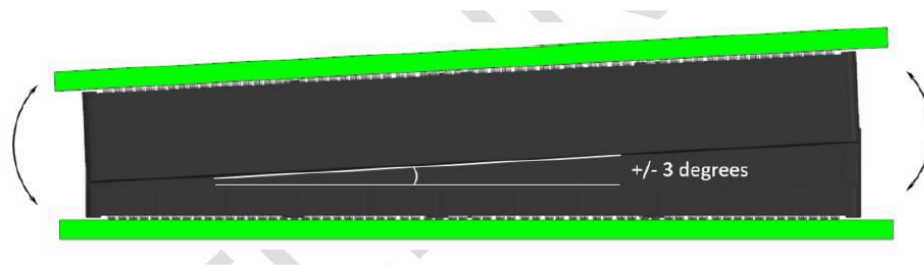


Figure 11-1: Module Removal

11.2 Flashing Operating System to the AGX Xavier Series Module

NOTE: The AGX Xavier Series Module must be programmed with the Diamond System Image file for the interfaces on the Stevie baseboard to be operational.

Diamond Systems Image is released as a compressed **tar.gz** file, that can be unzipped on a Linux Host Machine and flashed on to the AGX Xavier Series Module.

To update the image on the AGX Xavier Series Module, Stevie baseboard must be set to Recovery Mode. This is accomplished by pressing the **RCVRY (SW3)** button while powering up the baseboard.

Setting up the Hardware

1. Connect the USB A2A cable to the bottom port **J7** on the baseboard.
2. Connect the other end of the USB A2A cable to the Host PC.

After connecting the hardware:

3. Press the **RCVRY (SW3)** button while powering up the baseboard.

Refer to the following image for the location of the cable connections and to [Figure 6-2](#) for the location of the **RCVRY (SW3)** button.

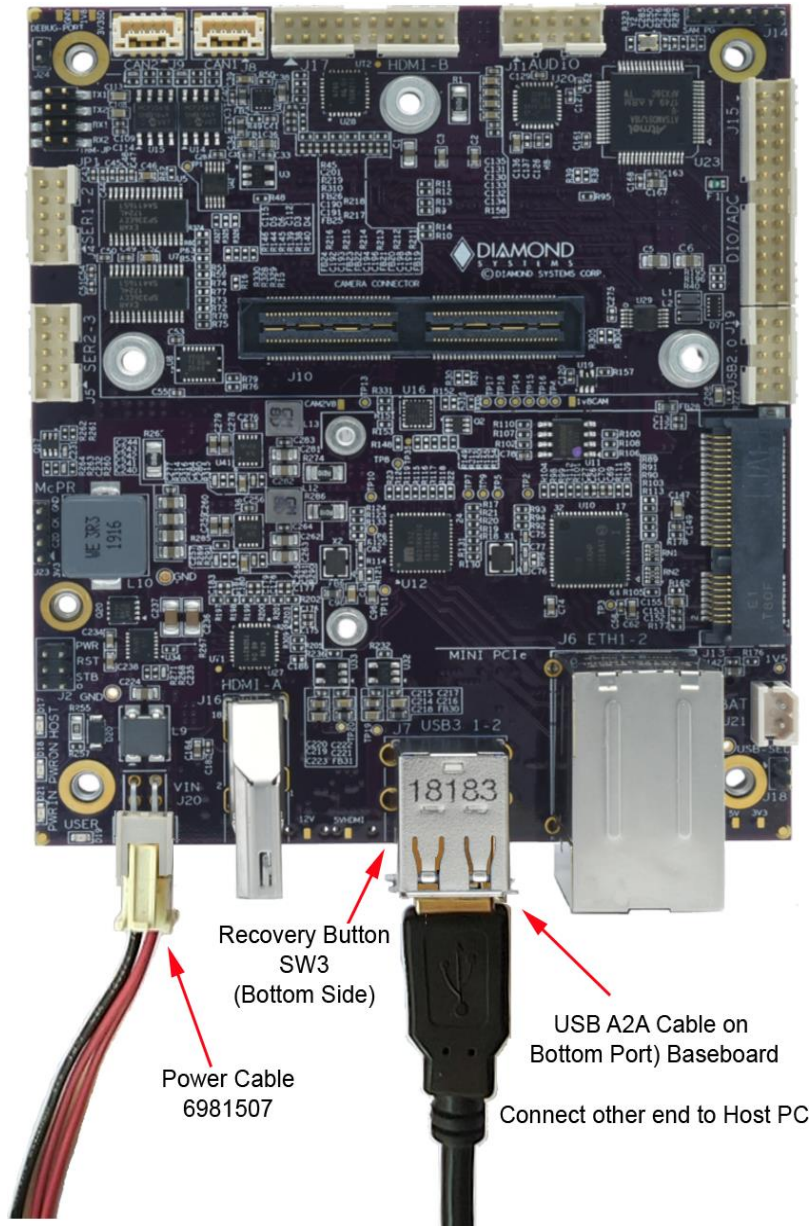


Figure 11-2: Setup to Initiate Recovery Mode on the Baseboard

NOTE: The sequence of images represented in this section have been captured from the Linux Host PC.

4. Download the Stevie baseboard Image file `Stevie-release-0.1-20190627.tar.gz` from the FTP (File Transfer Protocol) site and copy it to the Linux Host Machine.

```
donmichael@HMECD001406:~/xavier/release$ ls
elton-release-0.1-20190627.tar.gz
donmichael@HMECD001406:~/xavier/release$
```

Figure 11-3: Stevie Release Image File Displayed on Screen

To unzip the copied Image file:

5. Type and **Enter** the following command depicted in the Screen below. It may take a few minutes for the file to unzip.

```
sudo tar -pxvf stevie-release-0.1-20190627.tar.gz
```

NOTE: The tar .gz file name is liable to change according to the version and release date.

```
donmichael@HMECD001406:~/xavier/release$
donmichael@HMECD001406:~/xavier/release$ sudo tar -pxvf elton-release-0.1-20190627.tar.gz
```

Figure 11-4: Image File to be Extracted Screen

To switch to the directory where the file has been extracted:

6. Type and **Enter** the following command as depicted in the Screen below.

```
cd Linux_for_Tegra
```

```
donmichael@HMECD001406:~/xavier/release$
donmichael@HMECD001406:~/xavier/release$ ls
elton-release-0.1-20190627.tar.gz  Linux_for_Tegra
donmichael@HMECD001406:~/xavier/release$
donmichael@HMECD001406:~/xavier/release$ cd Linux_for_Tegra/
donmichael@HMECD001406:~/xavier/release/Linux_for_Tegra$
donmichael@HMECD001406:~/xavier/release/Linux_for_Tegra$ ls
apply_binaries.sh  jetson-xavier.conf          p2771-0000.conf.common      p2972-0000.conf.common      source_sync.sh
bootloader        jetson-xavier-maxn.conf     p2771-0000-devkit.conf     p2972-0000-devkit.conf
build_14t_bup.sh  jetson-xavier-slvs-ec.conf  p2771-0000-dsi-hdmi-dp.conf p2972-0000-devkit-maxn.conf
flash.sh          kernel                      p2771-3489-ucm1.conf       p2972-0000-devkit-slvs-ec.conf
jetson-tx2.conf   nv_tegra                   p2771-3489-ucm2.conf       rootfs
donmichael@HMECD001406:~/xavier/release/Linux_for_Tegra$
donmichael@HMECD001406:~/xavier/release/Linux_for_Tegra$
```

Figure 11-5: Image File Switch Directory Command Screen

To verify the baseboard is in Recovery Mode, in the Host PC running Ubuntu Operating System version 16.04 Terminal:

7. Type and **Enter**:

```
lsusb
```

The Terminal will display the NVIDIA device listed under USB devices as depicted below.

```
administrator@test:~$
administrator@test:~$ lsusb
Bus 001 Device 018: ID 0955:7c18 NVidia Corp.
Bus 001 Device 001: ID 1d6b:0002 Linux Foundation 2.0 root hub
Bus 005 Device 001: ID 1d6b:0001 Linux Foundation 1.1 root hub
Bus 004 Device 002: ID 093a:2510 Pixart Imaging, Inc. Optical Mouse
Bus 004 Device 001: ID 1d6b:0001 Linux Foundation 1.1 root hub
Bus 003 Device 001: ID 1d6b:0001 Linux Foundation 1.1 root hub
Bus 002 Device 002: ID 413c:2107 Dell Computer Corp.
Bus 002 Device 001: ID 1d6b:0001 Linux Foundation 1.1 root hub
administrator@test:~$
administrator@test:~$
```

Figure 11-6: Device Detected on NVidia USB Device

To flash the AGX Xavier Series Module:

8. Type and **Enter** the following:

```
sudo ./flash.sh jetson-xavier-maxn mmcblk0p1
```

The flashing process will take 15-20 minutes to complete.

NOTE: Do not interrupt or interfere with the USB connectivity or the power supply to Stevie until the flashing procedure is complete.

When the flashing is complete, the AGX Xavier Series Module will automatically Reboot.

On completion, a screen confirming a successful update to the Module will be displayed as shown below.

```

root@test: ~/Jethro_latest_image/Linux_for_Tegra
[ 188.7581 ] tegradevflash_v2 --write MB1_BCT mb1_cold_boot_bct_MB1_sigheader.bct.encrypt
[ 188.7594 ] Bootloader version 01.00.0000
[ 188.8352 ] Writing partition MB1_BCT with mb1_cold_boot_bct_MB1_sigheader.bct.encrypt
[ 188.8368 ] [.....] 100%
[ 188.9292 ]
[ 188.9316 ] tegradevflash_v2 --write MB1_BCT_b mb1_cold_boot_bct_MB1_sigheader.bct.encrypt
[ 188.9334 ] Bootloader version 01.00.0000
[ 189.0072 ] Writing partition MB1_BCT_b with mb1_cold_boot_bct_MB1_sigheader.bct.encrypt
[ 189.0088 ] [.....] 100%
[ 189.0758 ]
[ 189.0759 ] Flashing completed

[ 189.0760 ] Coldbooting the device
[ 189.0777 ] tegradevflash_v2 --reboot coldboot
[ 189.0791 ] Bootloader version 01.00.0000
[ 189.1605 ]
*** The target t186ref has been flashed successfully. ***
Reset the board to boot from internal eMMC.

root@test:~/Jethro_latest_image/Linux_for_Tegra#

```

Figure 11-7: Notification on Task Completion Screen

9. Power cycle the baseboard.
10. Remove the FORCE RECOVERY mode connections when powered OFF during power cycle.
11. Continue testing after system Restart.

12 DATA ACQUISITION (DAQ) SUBSYSTEM

12.1 SAM Data Acquisition Circuit

Overview

Stevie baseboard implements a data acquisition circuit with analog input, analog output, and digital I/O interfaces in conjunction with the NVidia Jetson AGX Xavier Series Module, which integrates a built-in DAQ subsystem supported by the Atmel SAM D51 Microcontroller Series Part No. [ATSAMD51J18A](#) from Microchip, to control and monitor “real world” devices.

A Programming Library provides resources for the development of custom applications along with a Graphical User Interface (GUI) that enables users to control the data acquisition I/O interface and data logging parameters.

Key features include:

- 6 Analog inputs, 0-3.3V input range, 12-bit resolution (1 part in 4096)
- 2 Analog outputs, 0-3.3V output range, 12-bit resolution (1 part in 4096)
- 13 Digital I/O (GPIO), 3.3V logic levels
- Miscellaneous board-specific controls

All DAQ I/Os are accessed on a 26-pin (2x13) 2mm pitch connector. Refer to Section: [8.12 Data Acquisition \(DAQ\) Connector: J15](#) for the pinout specifications.

The connector contains both analog and digital signals along with separate Grounds for each signal group. For noise cancellation procedures on the analog signals, all analog I/O connections must be referenced to the analog Ground pins 9 and 10, and all digital I/O signals must be referenced to the digital Ground pins 11 and 26.

A standard 2x13 2mm pitch ribbon cable connector or Diamond Systems non-latching cable No. 6980516 or latching cable No.6980606 can be plugged into the connector.

The Atmel SAM D51 microcontroller communicates with the AGX Xavier Series Module via a Serial Peripheral Interface (SPI) port. The SAM DAQ functions are controlled using the Programming Library included in the Stevie baseboard’s operating system image files.

Refer to [SAM D51 Software User Manual](#) located at Diamond Systems Corporate GitBook site for detailed information.

12.2 Analog Inputs

Analog Input sensors convert a voltage level signal into a digital value that can be analyzed, stored, and controlled.

The six analog inputs feature a 12-bit native resolution and single-ended 0-3.3V input range. The microcontroller is configured to use an external 3.3V reference voltage provided by a reference voltage IC on the board for improved accuracy.

<i>Analog Input</i>	
No. of Channels	6 Single-Ended or 3 Differential Inputs
Resolution	0x00112-bits (1 part in 4096) Native Up to 16-bits with Software Averaging
Input Voltage Range	0-3.3V
Sample rate	Maximum 1 KHz Using Diamond System Programming Library

Warning! There is no built-in protection circuitry on the analog inputs. Input voltages above the 3.3V maximum range may cause damage to the SAM microcontroller.

Although the native A/D resolution is 12-bits, the SAM microcontroller contains an innovative feature that enables higher resolution by averaging a number of samples. This technique enables the resolution to be configured to 16-bits.

Oversampling and averaging can be used to:

- Increase measurement resolution.
- Improve the Signal-to-Noise Ratio (SNR) and measurement resolution reduced throughput.
- Improve SNR for “white” noise.
- Reduce noise while maintaining a 12-bit resolution.

The disadvantages of averaging samples are an increased CPU utilization that results in each individual A/D measurement taking longer to compute and a reduced maximum sampling rate.

NOTE: Averaging is supported by the Programming Library.

The analog inputs can be configured in either single-ended or differential mode.

The pinouts for the mapping for input channels in differential mode are specified in [Table 13 5-1: I/O Signal Mapping](#).

For a single-ended input, the input voltage on the input pin is measured in comparison to the analog Ground pin on the I/O connector.

NOTE: It is recommended to avoid using the digital Ground pins for analog input measurements since it will display a higher noise-level and result in less accurate readings.

In a differential input, the voltage measurement is the value between the high and low input channels.

NOTE: In differential mode, the A/D value will not yield a measurement lower than 0V, corresponding to an A/D code of 0. In this scenario, the inputs may be considered to be “pseudo-differential”. A differential input is useful if the sensor or device being measured is far from the board or is powered by a different power supply wherein the Grounds of the two systems may differ.

A more accurate measurement can be obtained by connecting the Ground of the device being measured to the low channel on the SAM circuit, and the input signal to the high side.

The 12-bit resolution refers to the conversion of an analog voltage to a digital value in 12-bit integers.

The circuit can measure the input voltage with an accuracy of 3.3V / 4096 or approximately 0.81mV.

The conversion formulas between the input voltage and A/D code shown below, are based on the ideal case scenario.

A/D Conversion Formulas

$$\text{A/D code} = \text{input voltage} / 3.3\text{V} \times 4096 \text{ (min value 0, max value 4095)}$$

$$\text{Input voltage} = \text{A/D code} / 4096 \times 3.3\text{V}$$

The following table uses specific data for input voltage and A/D values based on the ideal case scenario.

NOTE: Based on convention, the top end of the 3.3V range should correspond to a code of 4096 which requires 13-bits. Therefore, the maximum A/D code of 4095 corresponds to 1 LSB less than 3.3V as shown in the following table.

<i>V_{in}</i>	<i>A/D Code Hex</i>	<i>A/D Code Dec</i>
0.0000V	0x000	0
0.0008V	0x001	1
0.0016V	0x002	2
0.0016V	0x002	
1.6592	0x7FF	2047
1.6500V	0x800	2048
1.6508V	0x801	2049
1.6508V	0x801	2049
3.2992V	0xFFF	4095

All A/D circuits are susceptible to inherent gain and offset errors depending upon factors such as temperature. The SAM circuit calibrates some of these errors to provide better accuracy.

The Diamond Systems driver and Programming Library calibrate raw uncorrected data or corrected data with greater accuracy between the A/D input range of 0V and/or 3.3V.

NOTE: Due to the inherent characteristics of the microcontroller regarding accuracy readings, the full input range of 0-3.3V may not be attainable.

In some scenarios, the minimum measurable voltage maybe a few millivolts above 0V, and the maximum measurable voltage maybe a few millivolts below 3.3V. In other scenarios, the corrected A/D measurement may exceed 0V or 3.3V.

This is due to software calculations which computes a straight line based on offset and gain calibration measurements. These extended voltage readings are correct.

A/D sampling can be performed one channel at a time or in a “scan” of multiple consecutive channels.

In a scan, a small-time delay exists between each sample, because the microcontroller converts the input voltages individually. The interval between the samples is approximately 1us. Additionally, interrupt processing can be used to manage a steady stream of A/D samples without the software monitoring each sample continuously.

A FIFO (First-In First-Out) in the SAM microcontroller stores A/D samples and forwards them to the main processor in chunks at regular intervals.

More details on A/D sampling methods can be found in the Programming Reference Manual.

12.3 Analog Outputs

Analog Output sensors convert digital values into analog voltages or current signals that can be analyzed and controlled.

A single-ended output is a signal that is always referenced to the shield -which is typically earth Ground, on the output connector. The voltage should be measured with respect to the analog Ground pins.

The two analog outputs feature a 12-bit resolution and single-ended 0-3.3V output range.

Analog Output	
No. of Channels	3 Single-Ended
Resolution	0x00112-bits (1 part in 4096) Native
Output Voltage Range	0-3.3V
Maximum Current	Refer to the SAM D5x/E5x Family Data Sheet for details.

NOTE: Do not use the digital Ground pins for analog output measurements since it has a higher noise-level and will result in poor quality output voltage signals.

The 12-bit resolution refers to the output of the requested voltage in 12-bit integers with an accuracy of 3.3V/4096 or approximately 0.81mV. The conversion formulas between D/A code and output voltage shown below are based on the ideal case scenario.

D/A Conversion Formulas

$$D/A \text{ code} = \text{desired output voltage} / 3.3V \times 4096 \text{ (min value 0, max value 4095)}$$

$$\text{Output voltage} = D/A \text{ code} / 4096 \times 3.3V$$

The following table uses specific data for input voltage and A/D values based on the ideal case scenario.

NOTE: Based on convention, the top end of the range (3.3V) must correspond to a code of 4096 which requires 13-bits. Therefore, the maximum D/A code of 4095 corresponds to 1 LSB less than 3.3V as specified in the table below.

D/A code Hex	D/A code Dec	Output voltage
0x000	0	0.0000V
0x001	1	0.0008V
0x002	2	0.0016V
0x7FF	2047	1.6592
0x800	2048	1.6500V
0x801	2049	1.6508V
0xFFE	4094	3.2984
0xFFF	4095	3.2992V

12.4 Digital I/O Operations

The DAQ circuit contains 13 digital I/O (GPIO) lines with 3.3V logic levels. During power-up or reset, all I/O lines are programmed to input direction to avoid any conflicts with external circuitry.

Each digital I/O line can be individually configured to set the input or output direction. This enables the lines to split between input and output. All lines can also be individually read or written or read in groups by port. Port A consists of 8 lines A0-A7, and Port B consists of 5 lines B0-B4.

12.5 Miscellaneous Functions

The SAM circuit administers several other circuits and features on the board. These features are controlled using the Programming Library that contains specifics on using the special-purpose I/O pins.

Power Supply Monitor

The SAM circuit uses four additional analog inputs to measure the on-board power supply voltages. In certain scenarios, the A/D reading needs to be multiplied by a scale factor to derive the actual voltage.

User LED Function

The circuit provides a LED connection tied to a GPIO line that is fully functional and can be controlled by the software to monitor the circuit.

Peripheral Control

The peripherals listed below are administered by the Atmel SAM D51 microcontroller. The available features vary from carrier board to board.

Refer to the Programming Reference Manual for details on each peripheral.

- Fan Enable/Disable (Connected to the fan connector)
- LTE Module Enable (Not applicable for Stevie)
- HDMI 5V Power Enable
- WLAN Disable
- Camera Power Control
- Serial Port Protocol Configuration

Temperature Monitor

The Atmel SAM D51 microcontroller contains a temperature monitor that reports the temperature of the chip in degrees Celsius. This is useful in obtaining information on the overall ambient temperature of the carrier board environment.

I/O Signal Mapping

NOTE: The specifications provided in the following table are for reference purposes only.

The pinout descriptions and their functions specified in the following table are derived from the Atmel SAM D51 Microcontroller Package No. TQFP-64 and are applicable when using the microcontroller.

The pinout specifications in the table do not apply to the Diamond Programming Library functions since the mapping functions are managed by the software.

Table 12.5-1: I/O Signal Mapping

<i>SAM Pin No.</i>	<i>SAM Pin Name</i>	<i>DAQ Function</i>
13	PA04 / ADC0_AIN4	ADC0 / ADC0-
12	PB09 / ADC0_AIN3	ADC1 / ADC0+
11	PB08 / ADC0_AIN2	ADC2 / ADC1-
16	PA07 / ADC0_AIN7	ADC3 / ADC1+
15	PA06 / ADC0_AIN6	ADC4 / ADC2-
64	PB03 / ADC0_AIN15	ADC5 / ADC2+
3	PA02 / DAC_VOUT0	DAC0
14	PA05 / DAC_VOUT1	DAC1
1	PA00	GPIO A0
63	PB02	GPIO A1
62	PB01	GPIO A2
61	PB00	GPIO A3
60	PB31	GPIO A4
59	PB30	GPIO A5
51	PA27	GPIO A6
50	PB23	GPIO A7
49	PB22	GPIO B0
46	PA25	GPIO B1
45	PA24	GPIO B2
44	PA23	GPIO B3
43	PA22	GPIO B4
17	PA08	5.0V Rail; Scale Factor 2.0
18	PA09	Main Input Voltage; Scale Factor 5.525
19	PA10	1.8V Rail; Scale Factor 1.0
20	PA11	3.3V Rail; Scale Factor 2.0
35	PA16	User LED
23	PB10	Fan enable
24	PB11	LTE module enable
39	PB16	HDMI 5.0V enable
40	PB17	WLAN disable#
36	PA17	Camera 1.2V enable (Active Low)
37	PA18	Camera 1.8V enable (Active High)
38	PA19	Camera 2.8V enable (Active High)
41	PA20	Serial Ports 1-2 Config bit 0
42	PA21	Serial Ports 1-2 Config bit 1
32	PA15	Serial Ports 1 & 2

13 SPECIFICATIONS

The Stevie baseboard specifications are summarized in the following table.

Feature	
Module	AGX Xavier Series
CPU	8-Core ARM v8.2 64-Bit CPU, 8MB L2 + 4 MB L3
SDRAM Memory	8/16/32 GB 256-bit LPDDR4x; 2133MHz – 137 GB/s
Display	Two Multi-Mode DP 1.2/eDP 1.4/HDMI 2.0
USB Ports	2x USB 2.0; 2x USB 3.1
Serial Ports	2 RS-232/422/485 Ports
DAQ	13 Digital I/Os 6x SE ADC Input or 3x DE ADC Input 2x DAC Output
Camera	4x MIPI CSI-2 x4 Lane Each
Connectivity	2 10/100/100 Mbps Ethernet, 1x NimbeLink Skywire® 4G LTE
Mass Storage	1 M.2 PCIe SSD, 1 Micro SD and UFS Card
Expansion Bus	1 Mini PCIe Full Size Card
Utility	PWR_BTN, RESET, FORCE RECOVERY
Digital/Analog Specifications	
Number of Lines	13
Direction	Programmable Bit by Bit
Input Voltage	
Logic 0:	0.0V Min, 0.99V Max, ±1uA
Logic 1	2.31V Min, 3.3V Max, ±1uA
Output Voltage	
Logic 0:	0.0V Min, 0.66V Max, +8mA (Typical)
Logic 1	2.64V Min, 3.3V Max, -8mA (Typical)
Analog Inputs	
Number of Inputs	6; Single-Ended or Differential
A/D Resolution	12-bit Resolution (1 Part in 4096);
Input Voltage Range	Single-Ended 0-3.3V
A/D sampling	One or Consecutive Channels
Analog Outputs	
Number of Outputs	2; Single-Ended
D/A Resolution	12-bit Resolution
Output Voltage Range	3.3V x 4096 (Min Value 0, Max Value 4095)
Mechanical and Environmental Properties	
System Input Voltage	+9VDC +/-5% to +20VDC +/-5%
Power Consumption	~30W
Dimensions	3.6" x 4.1" (92 mm x 105 mm)
Weight	TBU
Operating Temperature	-25°C To +80°C (-18°F To +176°F)
Shock	MIL-STD-202G Compatible
Vibration	MIL-STD-202G Compatible
RoHS	Compliant

14 ADDENDUM

The following section provides additional information and instructions relevant to the components specified in the Main Sections of this document.

14.1 Camera Installation Procedures

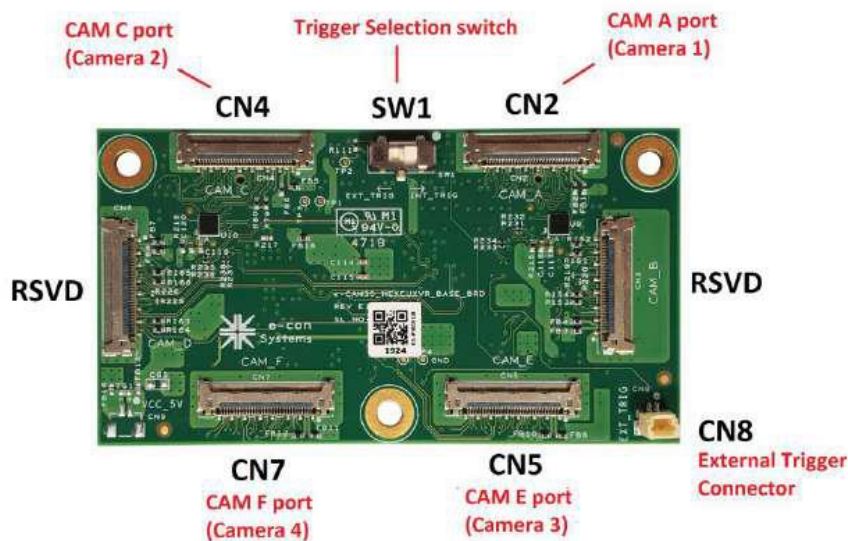
Like the Xavier Developer Kit Carrier Board, the Elton baseboard supports four MIPI CSI x4 camera interfaces through a 120-pin daughterboard connector.

Synchronized-4k-cameras from [e-con Systems™](#) can be plugged into the daughterboard connector to support the four 4-lane or six 2-lane cameras. The daughterboard connector also supports i2c and control signals which enable users to directly interface the camera to the baseboard.

The following procedures use the e-CAM130_CUXVR MIPI-four-AR1335-module camera board to demonstrate the installation and implementation of the cameras. The prebuild module drivers provided in the e-CAM130_CUXVR package are loaded automatically during the boot.

The e-CAM130_CUXVR is a multi-board set comprising of three board components as follows:

1. **The Camera Baseboard** (e-CAM30_HEXCUXVR_BASE_BRD)



Refer to the [e-CAM130_CUXVR_Getting_Started_Manual.pdf](#) on the [Documents](#) page located at the e-con Systems site for detailed interfacing information.

2. **The Adaptor Board** :
(e-CAM130_TRICUTX2_ADAPTOR)



3. **The Dual Board**
e-CAM137_CUMI1335_MOD

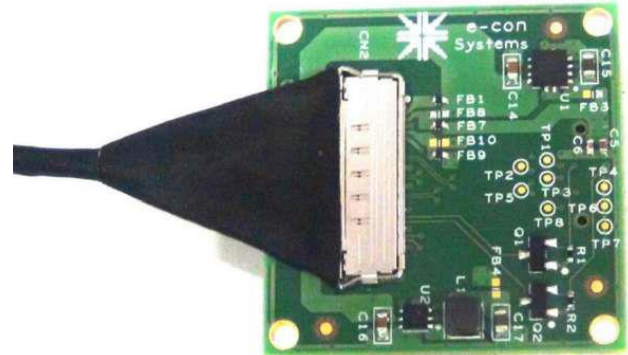


1. Insert the e-CAM130_CUXVR board CN1 connector to the camera connector on the Elton baseboard. Refer to Section 6: [Connector And Jumper Location](#). for the location of the camera connector.
2. Interface the four adaptor boards to the baseboard using the supplied four micro-coaxial cables.
3. Connect the micro-coaxial cable to the adaptor board connector and baseboard connector as depicted below.

The images of the micro-coaxial cable and the cable connected to the Adapter Board are shown below.



Micro-Coaxial Cable



Micro-Coaxial Cable Connected to Adaptor Board Connector

4. Lock the position of the cable on the baseboard.
5. Connect and lock the remaining three cameras as specified in Steps 1 through 4 above.

An image of the 4-camera installation is depicted below.



6. Power-On the system.

NOTE: For a successful implementation ensure that the trigger signal range conforms to 3.3V or 5V.

Voltage signals greater than 5V will cause permanent damage to the chip.

The synchronous mode is a special feature of the e-CAM130_CUXVR board that synchronizes all the captured camera frames according to the integrated PWM pulse within the trigger functionality. This PWM trigger pulses can be implemented internally using the Internal Trigger Mode, or externally using the External Trigger Mode.

7. Switch **SW1** to **EXT_TRIG** position when providing **PWM** trigger signal from an external source. When using an internal **PWM** trigger signal, the **SW1** switch must remain in the **INT_TRIG** position This calibrates frames in a synchronous mode.
8. Enter the following command line to access the cameras and begin the streaming process:

```
gst-launch-1.0 v4l2src device=/dev/video0 ! "video/x-raw,format=(string)UYVY, width=(int)3840, height=(int)2160" !
nvvidconv ! "video/x-raw(memory:NVMM),format=(string)I420,width=(int)1920, height=(int)1080" ! nvoverlaysink overlay-w=1920 overlay-h=1080
sync=false
```

When the command is executed the following screen will be displayed.

```
nvidia@jetson-0420119049088:~$ gst-launch-1.0 v4l2src device=/dev/video1 ! "video/x-raw,format=(string)UYVY, width=(int)3840, height=(int)2160" ! nvvidconv ! "video/x-raw(memory:NVMM),format=(string)I420,width=(int)1920, height=(int)1080" ! nvoverlaysink overlay-w=1920 overlay-h=1080 sync=false
Setting pipeline to PAUSED ...
Pipeline is live and does not need PREROLL ...
Setting pipeline to PLAYING ...
New clock: GstSystemClock
^Chandler interrupt.
Interrupt: Stopping pipeline ...
Execution ended after 0:00:03.837059981
Setting pipeline to PAUSED ...
Setting pipeline to READY ...
Setting pipeline to NULL ...
Freeing pipeline ...
nvidia@jetson-0420119049088:~$
```

9. To end the streaming process, enter **Ctrl + C** on the keyboard.
10. Enter the following command line to switch or change the parameters of the specific camera (1, 2, 3, or 4) respectively.
`device=/dev/video0 to 1,2,3,4.`

All camera streams can be viewed simultaneously using the integrated multi-camera features within the built-in application.

11. Enter the following command line to view all camera streams simultaneously within the terminal.
`./e-multicam.elf`

14.2 Serial Multiprotocol Configuration

Elton baseboard is equipped with four serial ports routed from the AGX Xavier Series Module through the programmable SP336 serial transceiver and implement selected RS232/422/485 protocols via GPIOs.

The SP336 is an integrated multiprotocol serial transceiver that contains both RS-232 and RS-485/RS-422 receivers and drivers and can be configured to operate in eight modes including RS-232-only (4Tx/4Rx), RS-485/RS-422-only (2Tx/2Rx) full or half-duplex, two RS-232/RS-485/RS-422 mixed-modes.

When configured in RS-485/RS-422 mode, each driver can be individually enabled for use on shared buses or bidirectional communication.

The SAM D51 microcontroller utility controls all four ports on the SP336 transceiver.

The microcontroller utility is used to set the modes for Ports 1 and 2 and the platform GPIOs are used to set the mode for Ports 3 and 4.

Launch the SAM microcontroller utility and set the mode as depicted in the screen below.

```
nvidia@jetson-0420119049088:~/Sam_Linux_64bit_CLI_Demos/DSCSAM_SerialPortConfig$ sudo ./DSCSAM_SerialPortConfig
[sudo] password for nvidia:
Board Type : ELTON

DSC SAM SERIAL PORT CONFIGURATION DEMO
Enter Serial Port Mode (0-RS232,1-RS422, 2-RS485):2
press Enter to repeat or 'q' to quit:q

DSC SAM Serial Port Configuration demo completed.
```

Figure 14-1: SAM Utility Serial Port Configuration

The RS485_util provides the option to enable or disable RS485/422 direction control on the UART ports.

NOTE: The RS485_util must be run after the ports are opened. Running the utility before the ports are open may result in the Terminal utility resetting the flag settings.

Before transmitting, set the mode for individual ports by replacing the -n parameter with the port number as shown in the syntax below.

```
#sudo rs485_util ttyTHS<n> 1
```

During transmission the RX protocol will be disabled.

After the transmission is complete the RX protocol will be enabled as depicted in the syntax and screen below.

```
#sudo rs485_util ttyTHS<n> 0
```

```
nvidia@jetson-0420119049088:~/Sam_Linux_64bit_CLI_Demos/DSCSAM_SerialPortConfig$ sudo rs485_util ttyTHS0 1
nvidia@jetson-0420119049088:~/Sam_Linux_64bit_CLI_Demos/DSCSAM_SerialPortConfig$
nvidia@jetson-0420119049088:~/Sam_Linux_64bit_CLI_Demos/DSCSAM_SerialPortConfig$
nvidia@jetson-0420119049088:~/Sam_Linux_64bit_CLI_Demos/DSCSAM_SerialPortConfig$ sudo rs485_util ttyTHS0 0
```

Figure 14-2: Enabled RX Protocol Screen

The table below lists the GPIO values and transceiver modes.

<i>Sysfs GPIO Number</i>	<i>RS232</i>	<i>RS422</i>	<i>RS485</i>
443	1	1	0
444	0	1	1

14.3 CAN Controller Configuration

The AGX Xavier Series Module integrate two independent CAN ports/channels which support connectivity to two CAN networks. The CAN interfaces `can0` and `can1` are routed to the Elton baseboard via CAN busses. The maximum speed that is supported is 1 mbps.

The CAN network driver provides a generic interface to setup, configure, and monitor CAN devices. The program `ip` is used to configure bit-timing parameters.

The following command line invokes the IP link to set the CAN bus bitrate before all operations begin.

```
sudo ip link set can0 type can bitrate 1000000
```

The following command line toggles the link up or down.

```
sudo ip link set up can0
```

The following command line sends CAN-frames via `CAN_RAW` sockets.

```
cansend can0 5A1#1122334455667788
```

The command `candump` dumps traffic on a CAN network. The following syntax shows the received message from the CAN bus.

```
candump can0
```

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- It is extended to the original Purchaser/Consumer.
- Under Terms and Conditions of the Warranty, Diamond Systems Corporation, at its sole discretion, will repair or replace any defective parts or components of its product.
- The product must be returned to Diamond Systems Corporation in the approved packaging, pre-authorized with a Diamond Systems Corporation-assigned Return Material Authorization (RMA) Number which is referenced on the shipping document.
- The Customer will prepay the shipment cost of the product to the Diamond Systems Corporation designated site.
- Diamond Systems Corporation will prepay the return shipping cost of the repaired or replaced the RMA product.

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